Lecture 6 MOSFET Small Signal Analysis

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MOSFET Small signal analysis

- Outline
  - 6.1 Small Signal Model of MOSFET
  - 6.2 Common Source (CS) Amplifier
  - 6.3 Common Gate (CG) Amplifier
  - 6.4 Common Drain or Source Follower Amplifier
  - 6.5 CMOS Digital Logic Inverter

Small Signal Models of MOSFET

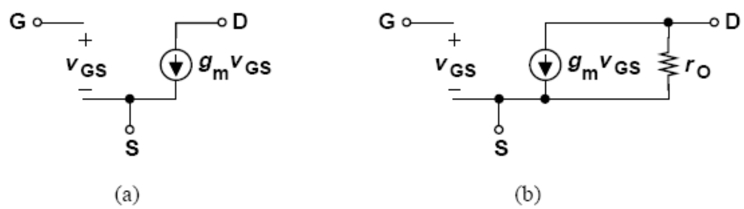


Figure 6.31 (a) Small-signal model of MOSFET, (b) inclusion of channel-length modulation.

MOS Transconductance

voltage-controlled current source,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

gm is linearly proportional to W/L

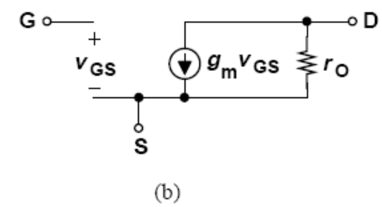
$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

gm is proportional to $\sqrt{W/L}$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

gm is linearly proportional to I_D

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$



g_m คือ ค่าถ่ายโอนความนำของมอสเฟต (Transconductance of MOSFET)

Model with Output Resistance

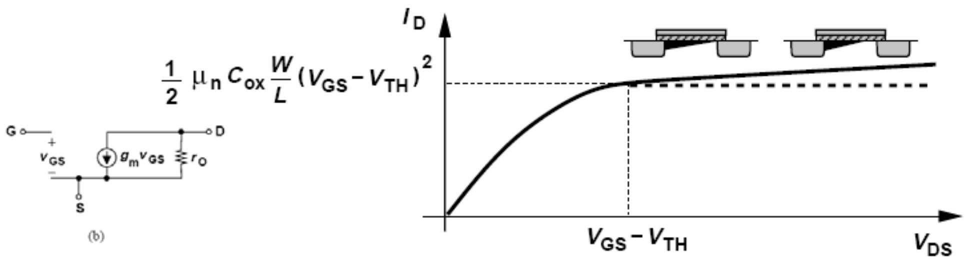


Figure 6.25 Variation of I_D in saturation region.

$$r_o = \frac{V_A}{I_D} \qquad V_A = \frac{1}{\lambda}$$

Including the effect of channel-length modulation modeled by output resistance

$$r_o = \frac{1}{\lambda I_D}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

r_o คือoutput impedance

Example 6.14

A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $W/L = 10$, and $\lambda = 0.1\ \text{V}^{-1}$, calculate its small-signal parameters.

Solution

We have

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{6.63}$$

$$= \frac{1}{1\ \text{k}\Omega}. \tag{6.64}$$

Also,

$$r_O = \frac{1}{\lambda I_D} \tag{6.65}$$

$$= 20\ \text{k}\Omega. \tag{6.66}$$

Example 6.16

For the configurations shown in Fig. 6.34(a), determine the small-signal resistances R_X and R_Y. Assume $\lambda \neq 0$.

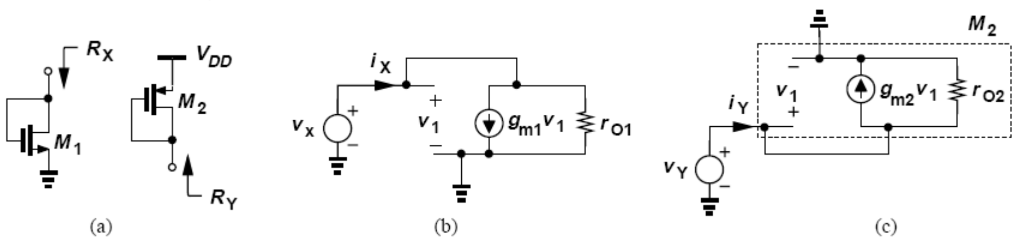


Figure 6.34 (a) Diode-connected NMOS and PMOS devices, (b) small-signal model of (a), (c) small-signal model of (b).

Solution

For the NMOS version, the small-signal equivalent appears as depicted in Fig. 6.34(b), yielding

$$R_X = \frac{v_X}{i_X} \tag{6.71}$$

$$= (g_{m1}v_X + \frac{v_X}{rO1})\frac{1}{i_X} \tag{6.72}$$

$$= \frac{1}{g_{m1}}||r_{O1}. \tag{6.73}$$

For the PMOS version, we draw the equivalent as shown in Fig. 6.34(c) and write

$$R_Y = \frac{v_Y}{i_Y} \tag{6.74}$$

$$= (g_{m2}v_Y + \frac{v_Y}{rO1})\frac{1}{i_Y} \tag{6.75}$$

$$= \frac{1}{g_{m2}}||r_{O2}. \tag{6.76}$$

In both cases, the small-signal resistance is equal to $1/g_m$ if $\lambda \to 0$.

In analogy with their bipolar counterparts [Fig. 4.44(a)], the structures shown in Fig. 6.34(a) are called "diode-connected" devices and act as two-terminal components: we will encounter many applications of diode-connected devices in Chapters 9 and 10.

MOSFET Amplifier

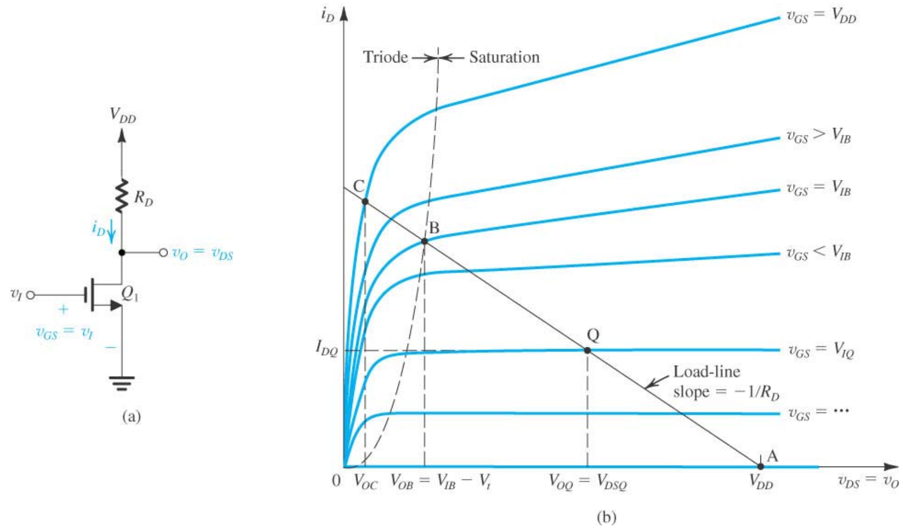
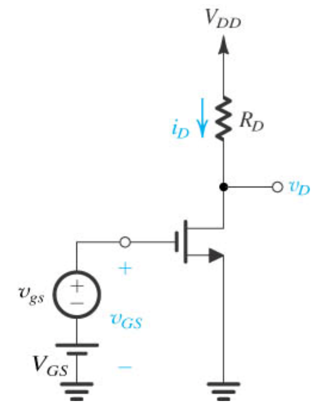


Figure 4.26 (a) Basic structure of the common-source amplifier. **(b)** Graphical construction to determine the transfer characteristic of the amplifier in (a).

MOSFET Amplifier



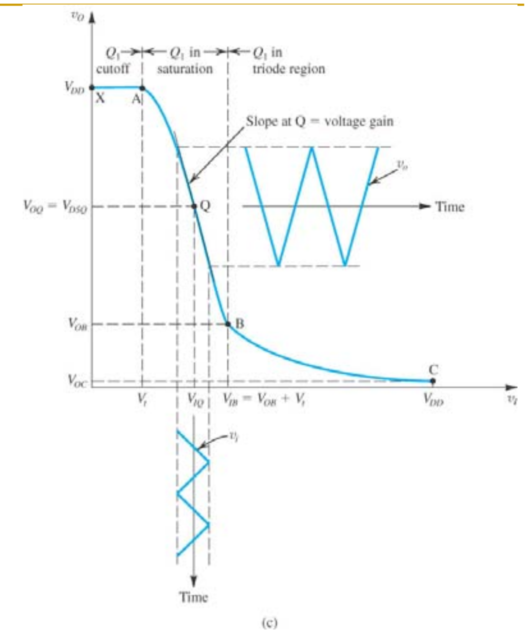
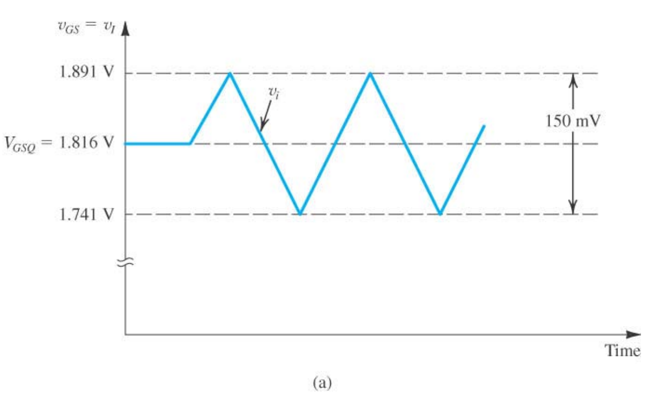


Figure 4.26 *(Continued)* **(c)** Transfer characteristic showing operation as an amplifier biased at point Q.

Input signal of amplifier circuit



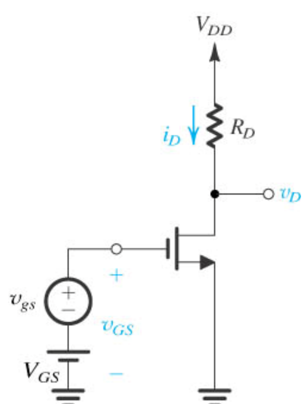
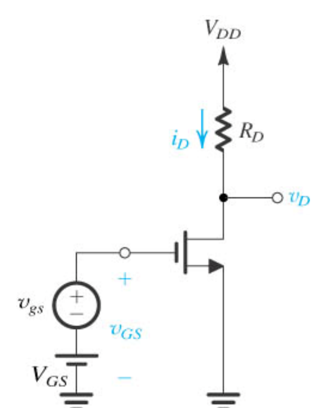
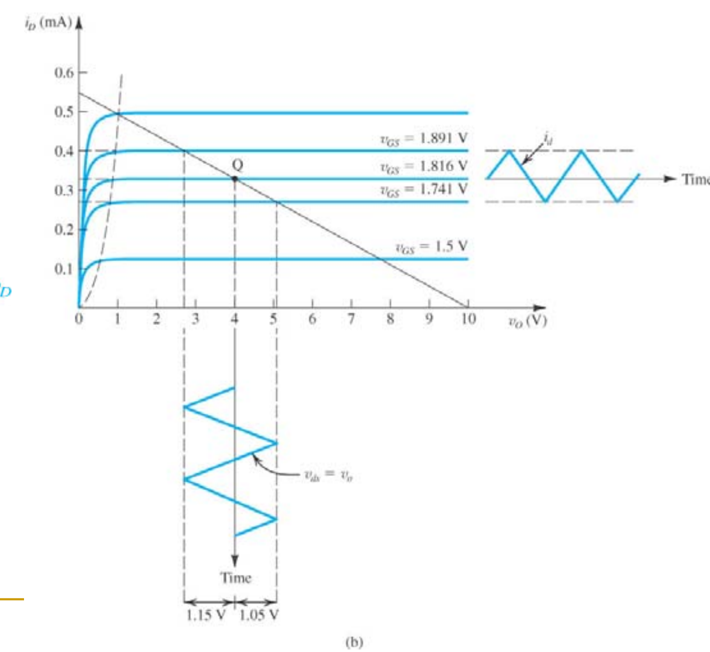


Figure 4.28 Example 4.8.

Output signal of amplifier circuit





Realization of Current Sources

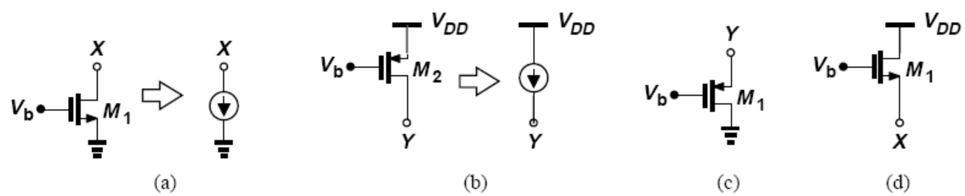
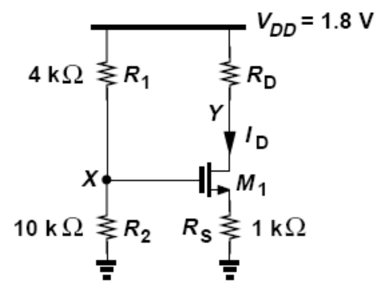


Figure 7.4 (a) NMOS device operating as a current source, (b) PMOS device operating as a current source, (c) PMOS topology not operating as a current source, (d) NMOS topology not operating as a current source.

Ex 1 Determine the bias current of M_1 in Fig. 7.1 assuming $\mu nCox = 100\ \mu A/V^2$, $V_{TH} = 0.5$ V, W/L = 5/0.18, and $\lambda = 0$. What is the maximum allowable value of R_D for M_1 to remain in saturation?



Ex 2 Determine the bias current of M_1 in Fig. assuming $K_n = 0.5\ mA/V^2$, $V_{TH} = 0.5$ V and $\lambda = 0$

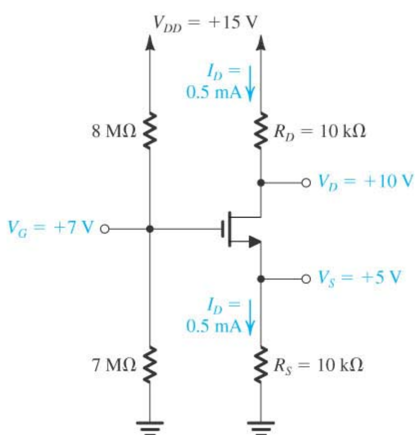
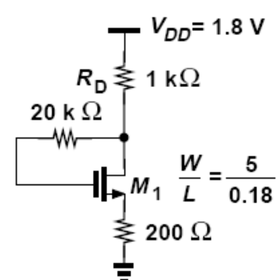


Figure 4.31 Circuit for Example 4.9.

Ex 3 Calculate the drain current of M_1 in Fig. 7.3 if $\mu nCox = 100\ \mu A/V^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$. What value of R_D is necessary to reduce I_D by a factor of two?



6.2 Common Source (CS) Amplifier

Small Signal Analysis

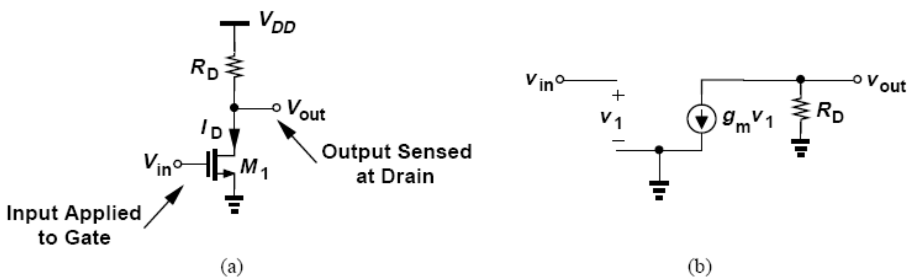
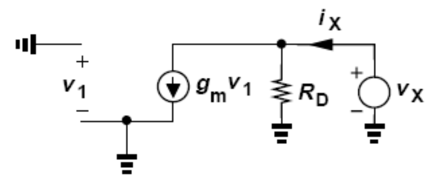


Figure 7.5 (a) Common-source stage, (b) small-signal mode.

$$A_v = -g_m R_D$$

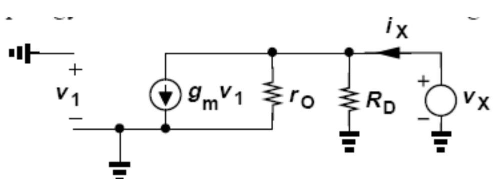
Output impedance without r_o



$$R_{in} = \infty$$

$$R_{out} = R_D$$

Output impedance include r_o



$$A_v = -g_m\left(r_o // R_D\right)$$

$$R_{in} = \infty$$

$$R_{out} = r_o // R_D$$

Example 7.4

Calculate the small-signal voltage gain of the CS stage shown in Fig. 7.6 if $I_D = 1$ mA, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$. Verify that M_1 operates in saturation.

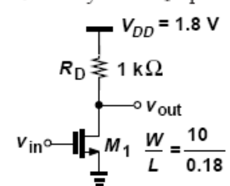


Figure 7.6 Example of CS stage.

Solution

We have

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{7.38}$$

$$= \frac{1}{300\ \Omega}. \tag{7.39}$$

Thus,

$$A_v = -g_m R_D \tag{7.40}$$

$$= 3.33. \tag{7.41}$$

To check the operation region, we first determine the gate-source voltage:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{7.42}$$

$$= 1.1\ \text{V}. \tag{7.43}$$

The drain voltage is equal to $V_{DD} - R_D I_D = 0.8$ V. Since $V_{GS} - V_{TH} = 0.6$ V, the device indeed operates in saturation and has a margin of 0.2 V with respect to the triode region. For example, if R_D is doubled with the intention of doubling A_v, then M_1 enters the triode region and its transconductance drops.

CS Stage with Degeneration

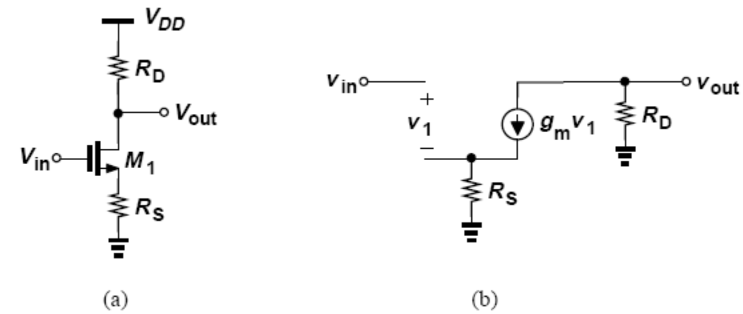


Figure 7.14 (a) CS stage with degeneration, (b) small-signal model.

$$v_{in} = v_1 + g_m v_1 R_S \tag{7.64}$$

and hence

$$v_1 = \frac{v_{in}}{1 + g_m R_S}. \tag{7.65}$$

Since $g_m v_1$ flows through R_D, $v_{out} = -g_m v_1 R_D$ and

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} \tag{7.66}$$

$$= -\frac{R_D}{\frac{1}{g_m} + R_S}, \tag{7.67}$$

a result identical to that expressed by (5.157) for the bipolar counterpart.

CS Core with Biasing

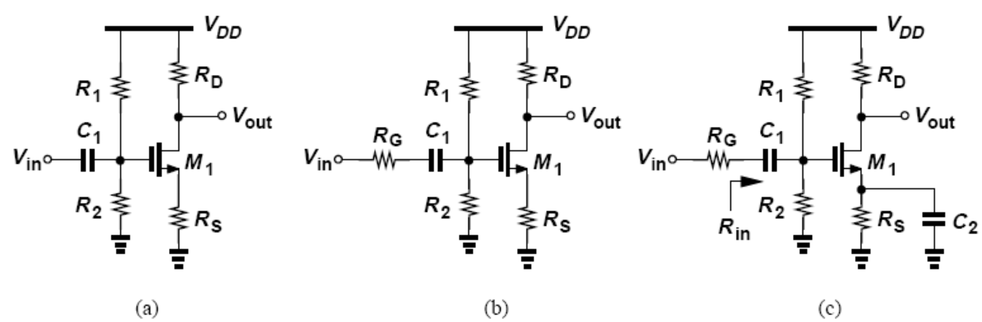


Figure 7.20 (a) CS stage with input coupling capacitor, (b) inclusion of gate resistance, (c) use of bypass capacitor.

$$R_{in} = R_1 || R_2. \quad (7.79)$$

Thus, if the circuit is driven by a finite source impedance [Fig. 7.20(b)], the voltage gain falls to

$$A_v = \frac{R_1||R_2}{R_G + R_1||R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, \quad (7.80)$$

where λ is assumed to be zero.

As mentioned in Chapter 5, it is possible to utilize degeneration for bias point stability but eliminate its effect on the small-signal performance by means of a bypass capacitor [Fig. 7.20(c)]. Unlike the case of bipolar realization, this does not alter the input impedance of the CS stage:

$$R_{in} = R_1 || R_2, \quad (7.81)$$

but raises the voltage gain:

$$A_v = -\frac{R_1||R_2}{R_G + R_1||R_2} g_m R_D. \quad (7.82)$$

6.3. Common Gate (CG) Amplifier

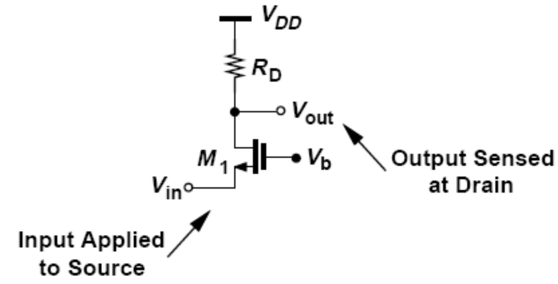


Figure 7.21 Common-gate stage.

$$A_v = g_m R_D$$

Input impedance and Output impedance

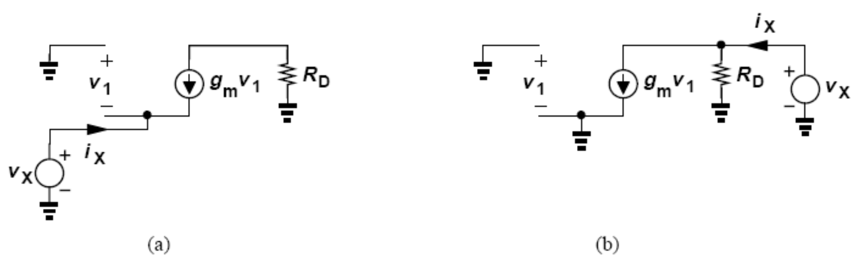


Figure 7.23 (a) Input and (b) output impedances of CG stage.

$$R_{in} = \frac{1}{g_m}$$

$$R_{out} = R_D$$

Input impedance

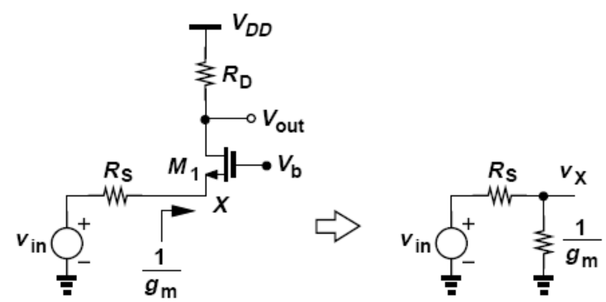


Figure 7.24 Simplification of CG stage with signal source resistance.

$$v_X = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} v_{in} \quad (7.105)$$

$$= \frac{1}{1 + g_m R_S} v_{in}. \quad (7.106)$$

Thus,

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_X} \cdot \frac{v_X}{v_{in}} \quad (7.107)$$

$$= \frac{g_m R_D}{1 + g_m R_S} \quad (7.108)$$

$$= \frac{R_D}{\frac{1}{g_m} + R_S}. \quad (7.109)$$

Output impedance

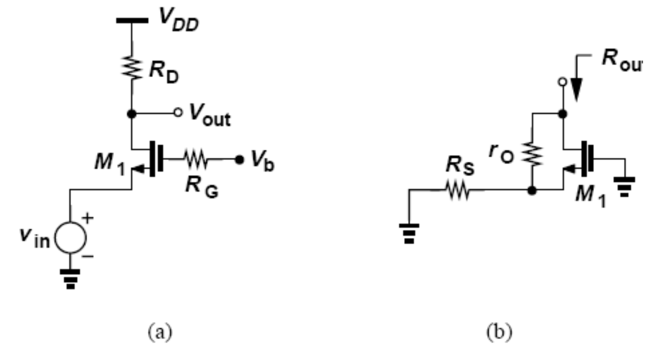


Figure 7.25 (a) CG stage with gate resistance, (b) output resistance of CG stage.

$$R_{out} = (1 + g_m r_O) R_S + r_O.$$

CG Stage with Biasing

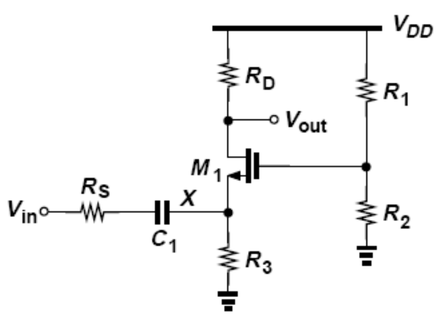


Figure 7.27 CG stage with biasing.

Since the impedance seen to the right of node X is equal to $R_3||(1/g_m)$, we have

$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X} \quad (7.118)$$

$$= \frac{R_3||(1/g_m)}{R_3||(1/g_m) + R_S} \cdot g_m R_D, \quad (7.119)$$

where channel-length modulation is neglected. As mentioned earlier, the voltage divider consisting of R_1 and R_2 does not affect the small-signal behavior of the circuit (at low frequencies).

6.4. Common Drain or Source Follower Amplifier

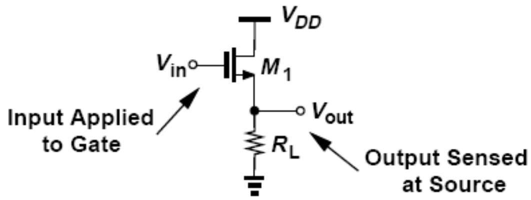


Figure 7.28 Source follower.

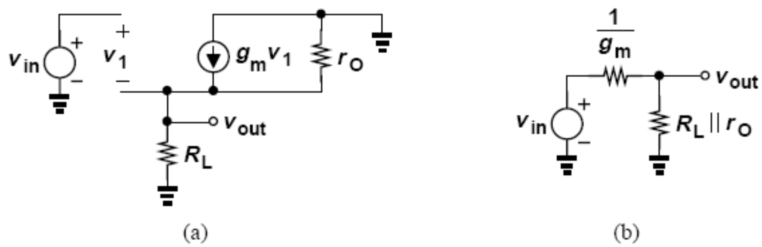


Figure 7.29 (a) Small-signal equivalent of source follower, (b) simplified circuit.

Figure 7.29(a) depicts the small-signal equivalent of the source follower, including channel-length modulation. Recognizing that r_O appears in parallel with R_L, we have

$$g_m v_1 (r_O || R_L) = v_{out}. \qquad (7.128)$$

Also,

$$v_{in} = v_1 + v_{out}. \qquad (7.129)$$

It follows that

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O || R_L)}{1 + g_m (r_O || R_L)} \qquad (7.130)$$

$$= \frac{r_O || R_L}{\frac{1}{g_m} + r_O || R_L}. \qquad (7.131)$$

Output impedance of the source follower.

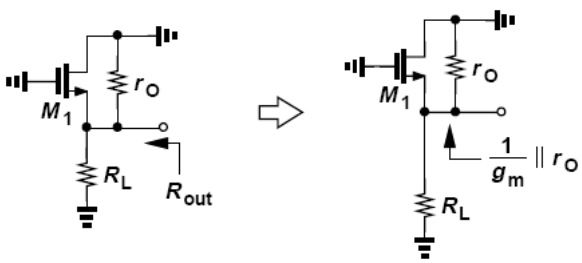


Figure 7.31 Output resistance of source follower.

$$R_{out} = \frac{1}{g_m} || r_O || R_L \qquad (7.136)$$

$$\approx \frac{1}{g_m} || R_L. \qquad (7.137)$$

Source Follower with Biasing

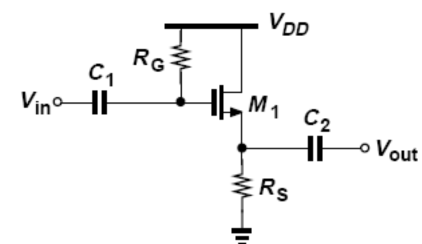


Figure 7.32 Source follower with input and output coupling capacitors.

CMOS Technology

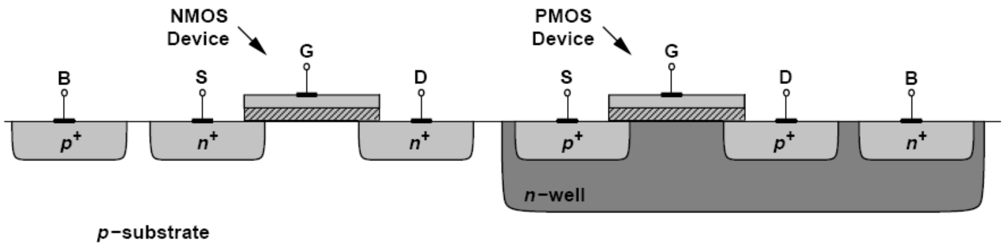
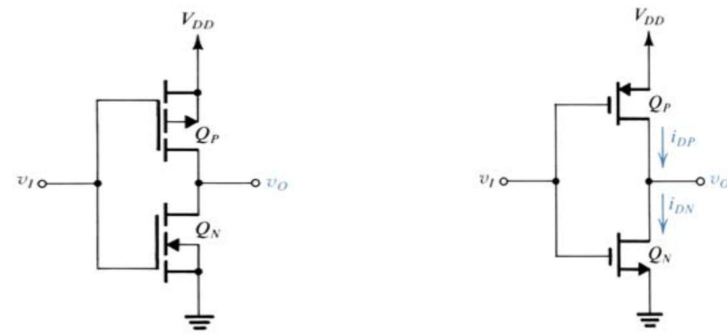


Figure 6.35 CMOS technology.

The CMOS inverter

Simplified circuit schematic for the inverter.



Comparison of Bipolar and MOS Devices

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
−	Voltage−Dependent Resistor

Table 6.2 Comparison of bipolar and MOS transistors.

Ex The CMOS inverter

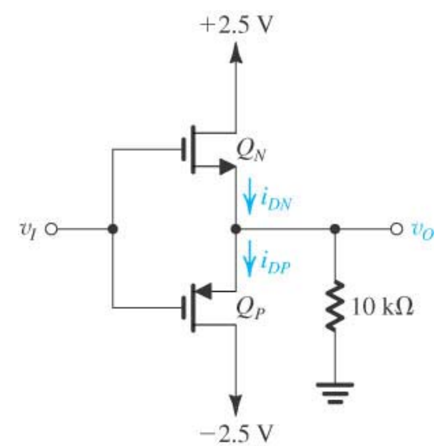


Figure E4.16

The CMOS inverter analysis

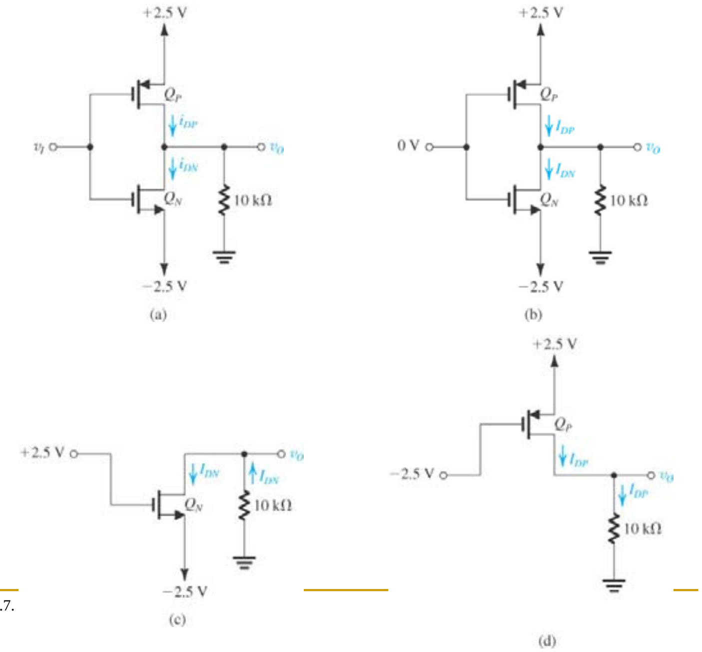


Figure 4.25 Circuits for Example 4.7.

Voltage transfer characteristic of the CMOS inverter.

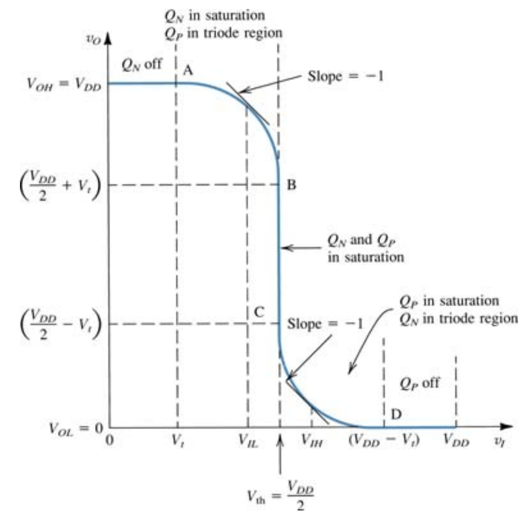


Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

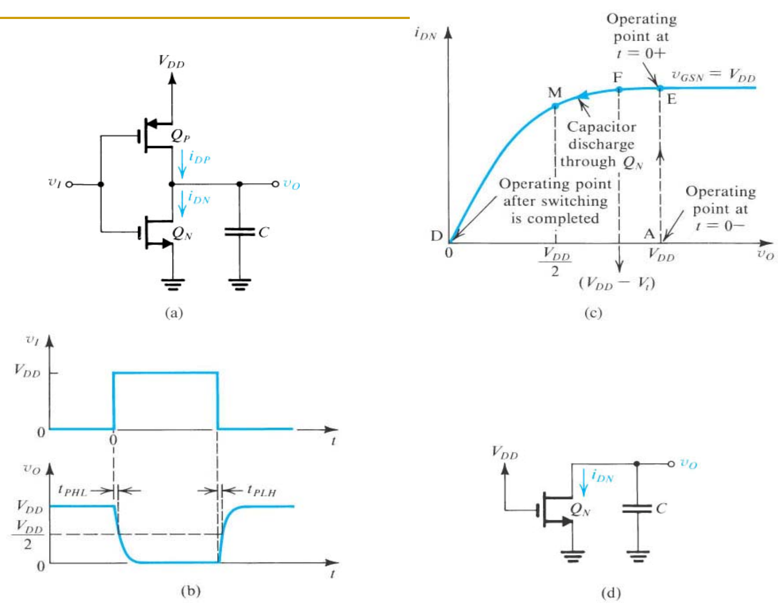
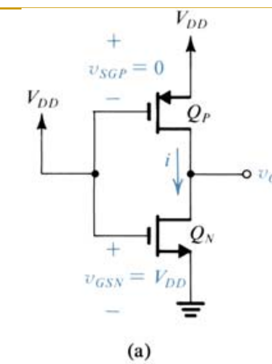
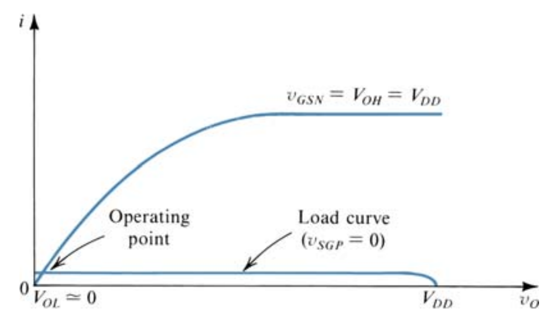
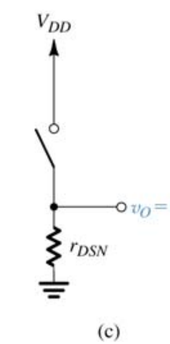


Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N; **(d)** equivalent circuit during the capacitor discharge.

CMOS inverter operation

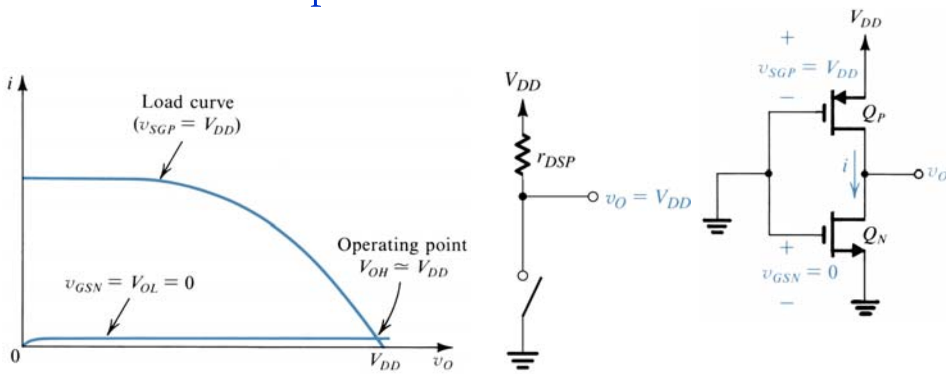






v_1 is high: (a) circuit with $v_1 = V_{DD}$ (logic-1 level, or V_{OH}); (b) graphical construction to determine the operating point; and (c) equivalent circuit.

CMOS inverter operation



(c)

v_1 is low: graphical construction to determine the operating point; and (c) equivalent circuit.

เอกสารอ้างอิง (Reference)

1. Behzad Razavi “Fundamentals of Microelectronics”
2. Adel S. Sedra, Kenneth C. Smith “Microelectronic Circuit”
3. Pual R. Gray and Robert G. Mayer “Analysis and Design of Integrated Circuit”
4. รศ.สักรียา ชิตวงศ์ “วิศวกรรมอิเล็กทรอนิกส์”

Thank you