Lecture 5 MOSFET

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Outline

- 5.1 Structure and Physical Operation of the Enhancement-Type MOSFET
- 5.2 Current-Voltage Characteristic of the Enhancement MOSFET
- 5.3 MOSFET Circuit at DC
- 5.4 The MOSFET as an Amplifier
- 5.5 Biasing in MOS Amplifier Circuits

Field Effect (MOS) Transistor

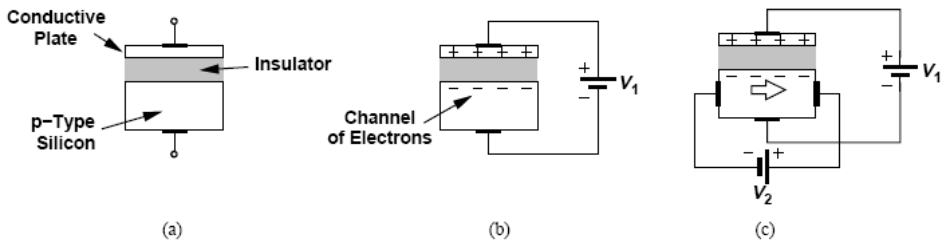
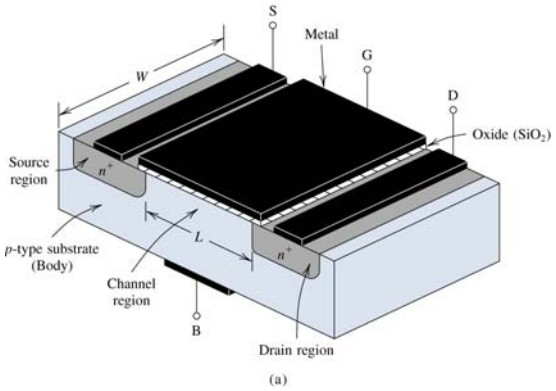
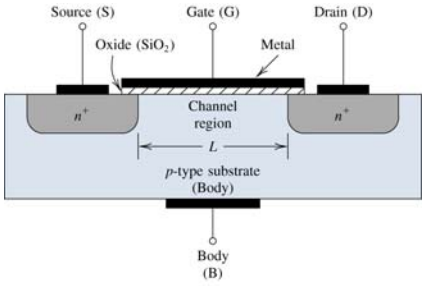


Figure 6.1 (a) Hypothetical semiconductor device, (b) operation as a capacitor, (c) current flow as a result

Field Effect (MOS) Transistor





Typically L = 1 to 10 μm, W = 2 to 500 μm, and the thickness of the oxide layer is in the range of 0.02 to 0.1 μm.

Structure of MOSFET

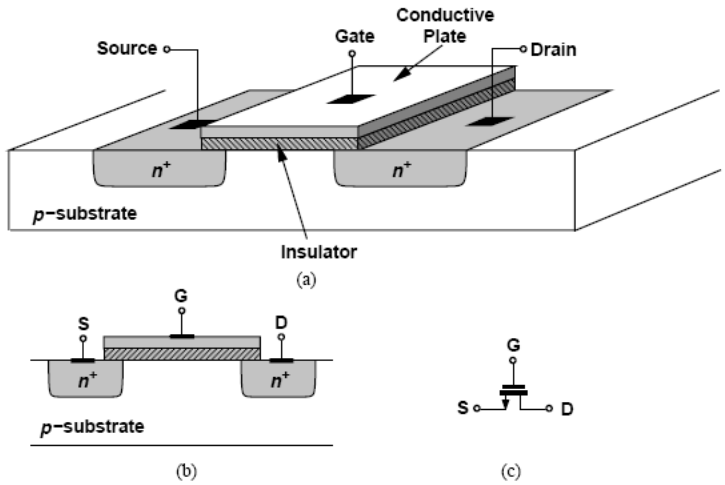
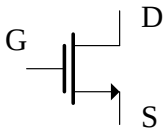
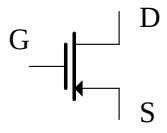


Figure 6.2 (a) Structure of MOSFET, (b) side view, (c) circuit symbol.

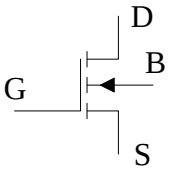
Symbol of MOSFET

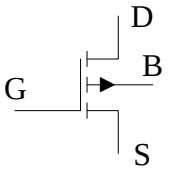


n-channel enhancement-type MOSFET



p-channel enhancement-type MOSFET





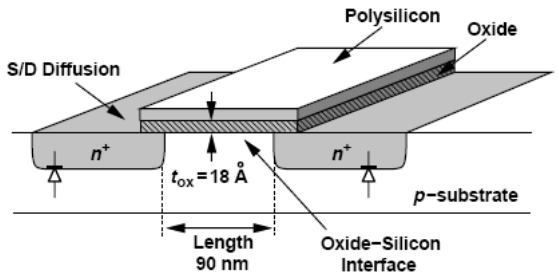


Figure 6.3 Typical dimensions of today's MOSFETs.

MOSFET with gate voltage

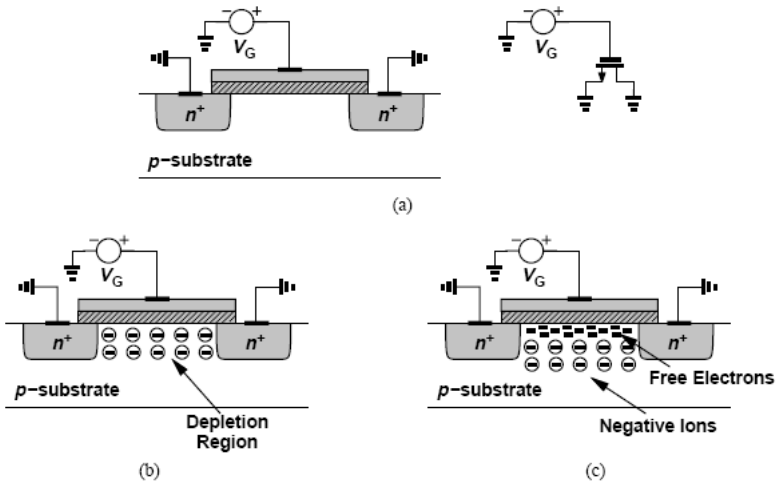


Figure 6.5 (a) MOSFET with gate voltage, (b) formation of depletion region, (c) formation of channel.

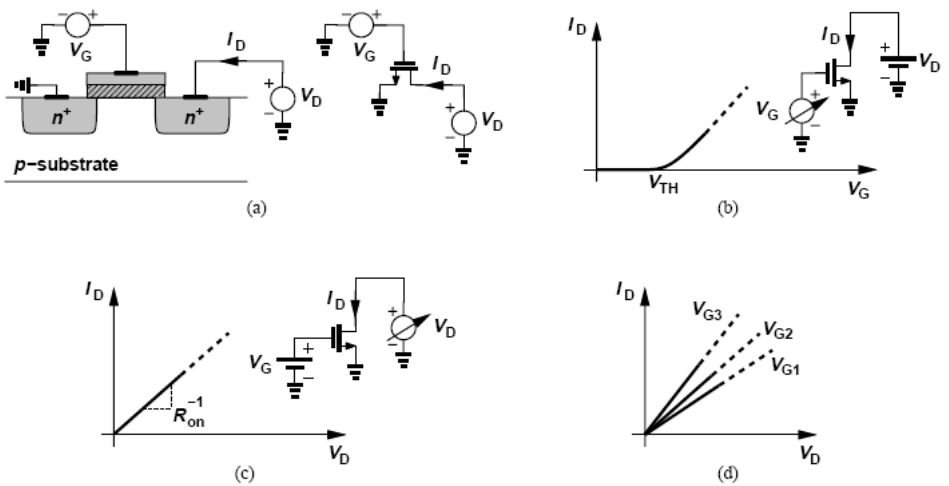


Figure 6.8 (a) MOSFET with gate and drain voltages, (b) I_D-V_G characteristic, (c) I_D-V_D characteristic, (d) I_D-V_D characteristics for various gate voltages .

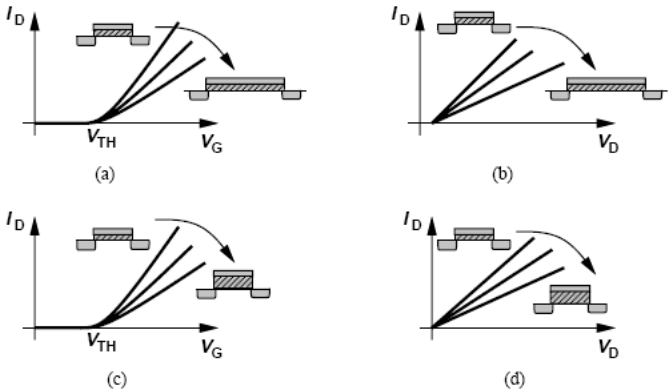


Figure 6.9 (a) I_D-V_G characteristics for different channel lengths, (b) I_D-V_D characteristics for different channel lengths, (c) I_D-V_G characteristics for different oxide thicknesses, (d) I_D-V_D characteristics for different oxide thicknesses.

t_{ox} cannot.

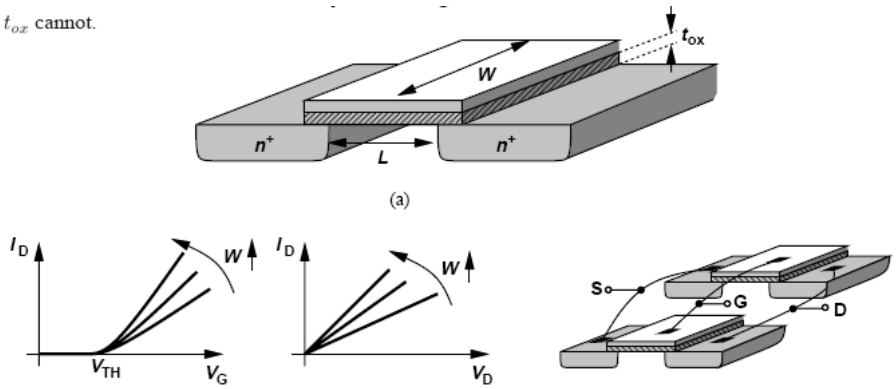


Figure 6.10 (a) Dimensions of a MOSFET (W and L are under circuit designer's control.), (b) I_D characteristics for different values of W, (c) equivalence to devices in parallel.

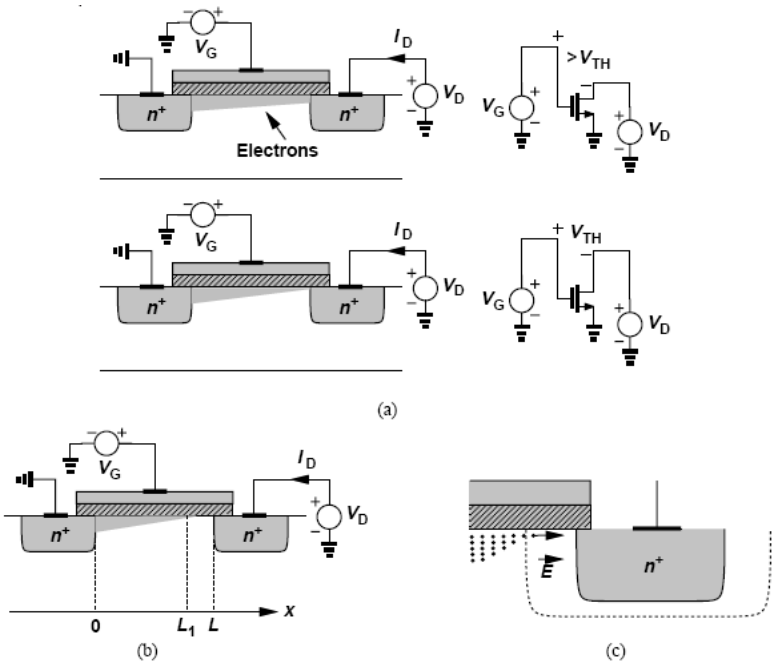
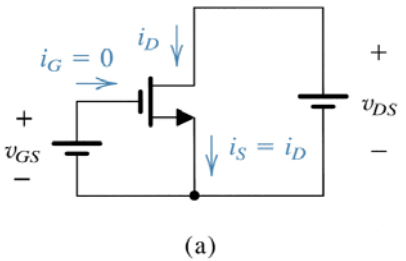
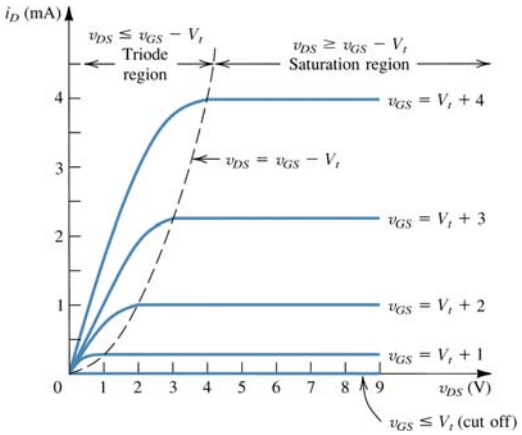


Figure 6.12 (a) Pinchoff, (b) variation of length with drain voltage, (c) detailed operation near the drain.

n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow





The i_D - v_{DS} characteristics for a device with V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2.

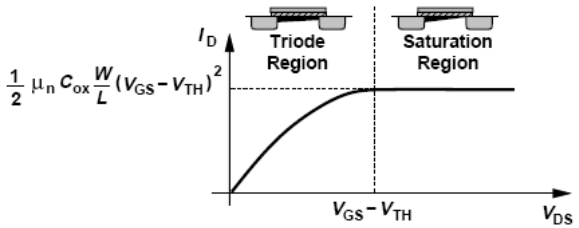


Figure 6.21 Overall MOS characteristic.

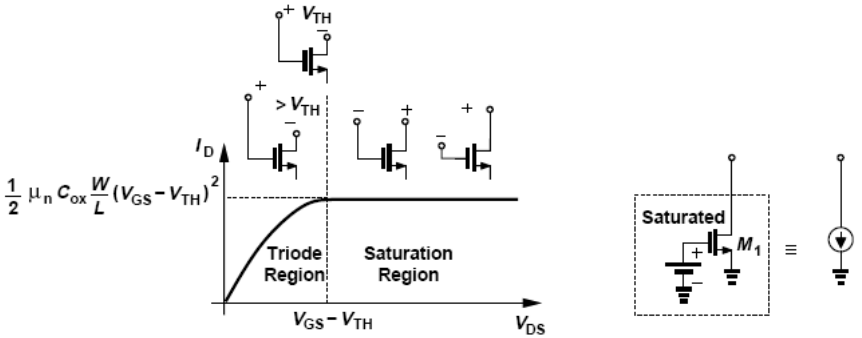
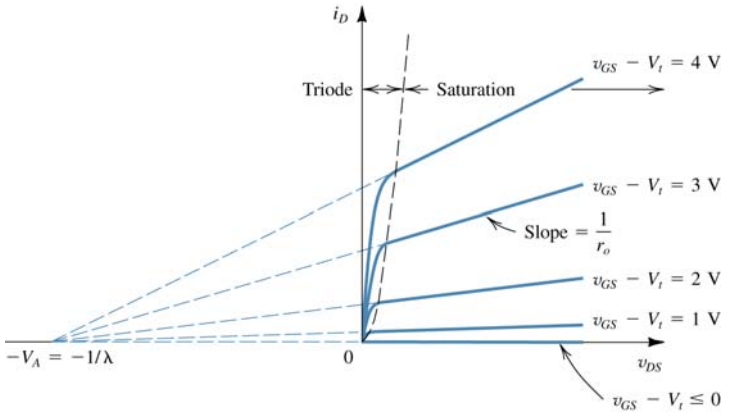


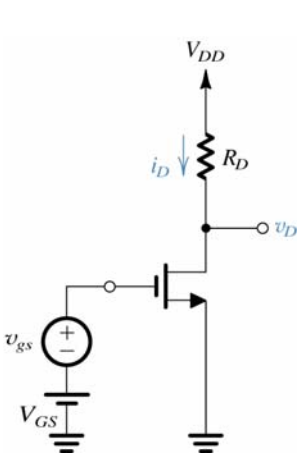
Figure 6.22 Illustration of triode and saturation regions based on the gate and drain voltages.

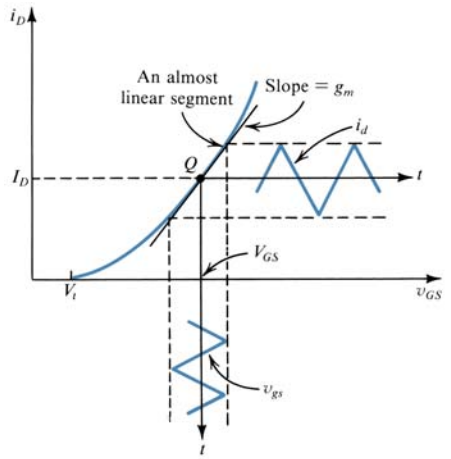
Effect of v_{DS} on i_D in the saturation region.



The MOSFET parameter V_A is typically in the range of 30 to 200 V.

MOSFET as an amplifier.

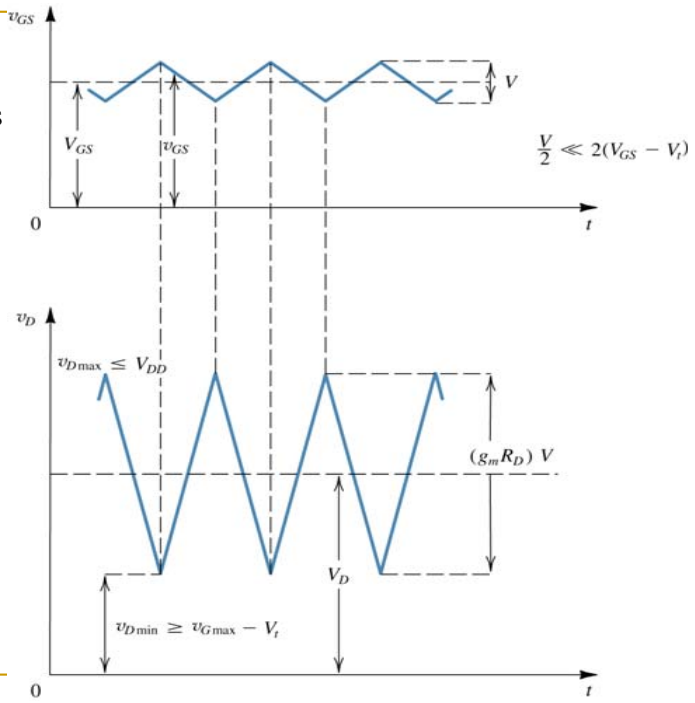




Small Signal

Instantaneous voltages

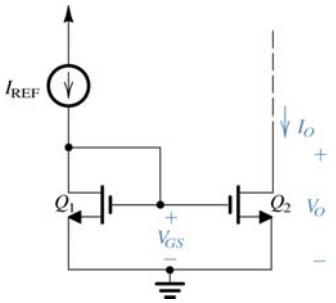
v_{GS} and v_D

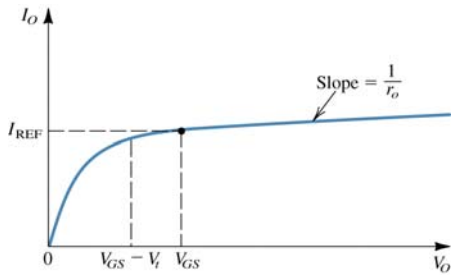


Sample Circuit

MOSFET current mirror.

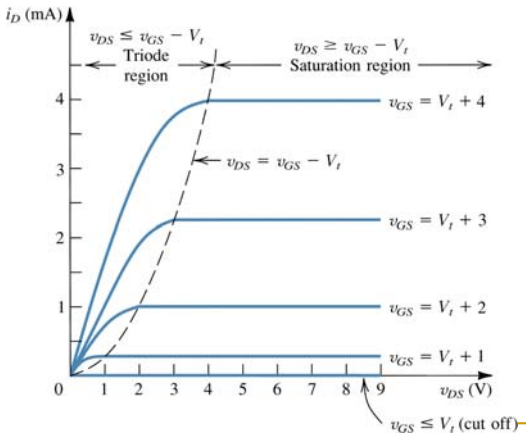
Output characteristic of the current current mirror Q_2 is matched to Q_1.





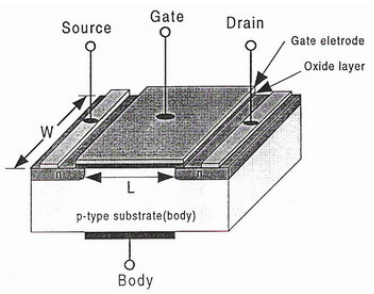
5.1 Current-Voltage Characteristic of enhancement MOSFET

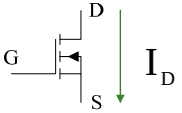
Current-Voltage Characteristic of enhancement MOSFET



- 1. MOSFET ไม่ทำงาน (Cutoff Region)
- 2. MOSFET ทำงานในช่วงไม่อิ่มตัว (Non-Saturation Region) หรือช่วงเชิงเส้น (Linear Region) หรือ (Triode Region)
- 3. MOSFET ทำงานในช่วงอิ่มตัว (Saturation Region)

5.2 DC Bias MOSFET

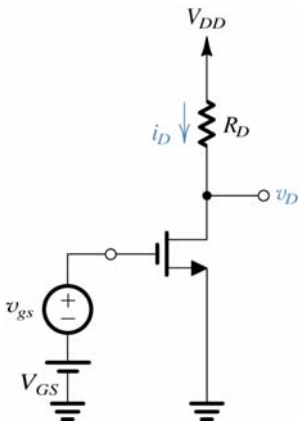




$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- โดยที่
- μ_n = ค่าสภาพความคล่องตัวของโฮลหรืออิเล็กตรอนที่ผิว (Surface Mobility of Carrier)
- C_{OX} = ค่าความจุไฟฟ้าต่อพื้นที่ของเกทออกไซด์ (Capacitance per unit area of the gate)
- W = ความกว้างของแชลแนล (Channel Width)
- L = ความยาวของแชลแนล (Channel Length)
- V_{GS} = แรงดันไฟฟ้าระหว่างเกตกับซอส (Gate-Source Voltage)
- V_{DS} = แรงดันไฟฟ้าระหว่างเดรนกับซอส (Drain-Source Voltage)
- V_{th} = แรงดันขีดเริ่ม (Threshold Voltage)
- I_D = กระแสเดรน (Drain Current)

DC Bias MOSFET (con)



- 1. MOSFET ไม่ทำงาน (Cutoff Region)

$$I_D = 0 \qquad V_{GS} < V_{th}$$

- 2. MOSFET ทำงานในช่วงไม่อิ่มตัว (Non-Saturation Region) หรือช่วงเชิงเส้น (Linear Region) หรือ (Triode Region)

$$I_D = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{th})V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$V_{GS} > V_{th} \qquad 0 < V_{DS} < (V_{GS}-V_{th})$$

DC Bias MOSFET (Con)

$$I_D \cong \mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_{th})V_{DS}$$

$$V_{GS} > V_{th} \qquad 0 < V_{DS} << (V_{GS}-V_{th})$$

$$R_{DS} = \frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_{th})}$$

- 3. MOSFET ทำงานในช่วงอิ่มตัว (Saturation Region)

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$$

$$k_n' = \frac{1}{2}\mu_n C_{ox}$$

$$I_D = k_n'\frac{W}{L}(V_{GS}-V_t)^2$$

$$K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

$$\boxed{I_D = K_n(V_{GS}-V_t)^2}$$

Example 6.6

Calculate the bias current of M_1 in Fig. 6.23. Assume $\mu_n C_{ox} = 100\ \mu A/V^2$ and $V_{TH} = 0.4$ V. If the gate voltage increases by 10 mV, what is the change in the drain voltage?

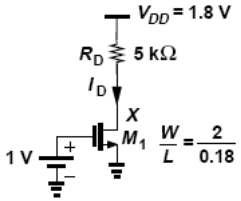


Figure 6.23 Simple MOS circuit.

Solution

It is unclear a priori in which region M_1 operates. Let us assume M_1 is saturated and proceed. Since $V_{GS} = 1$ V,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \qquad (6.18)$$

$$= 200\ \mu A. \qquad (6.19)$$

We must check our assumption by calculating the drain potential:

$$V_X = V_{DD} - R_D I_D \qquad (6.20)$$

$$= 0.8\ \text{V}. \qquad (6.21)$$

The drain voltage is lower than the gate voltage, but by less than V_{TH}. The illustration in Fig. 6.22 therefore indicates that M_1 indeed operates in saturation.

If the gate voltage increases to 1.01 V, then

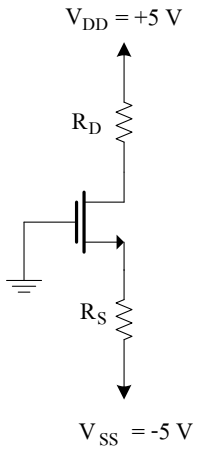
$$I_D = 206.7\ \mu A, \qquad (6.22)$$

lowering V_X to

$$V_X = 0.766\ \text{V}. \qquad (6.23)$$

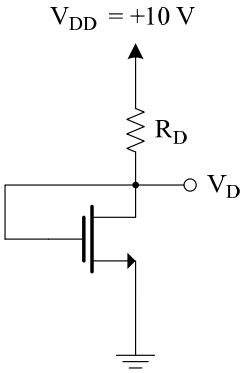
Fortunately, M_1 is still saturated. The 34-mV change in V_X reveals that the circuit can *amplify* the input.

Ex 5.1 Design the circuit of figure at I_D = 0.4 mA and V_D = +1 V. The NMOS transistor has V_t = 2 V $K_n = k_n'(W/L) = 0.4mA/V^2$

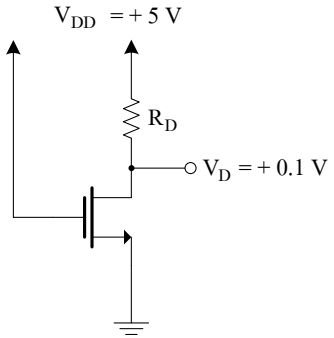


Ex 5.2 Design the circuit of figure at I_D = 0.4 mA. Find value R and dc voltage V_D. The NMOS transistor has V_t = 2 V

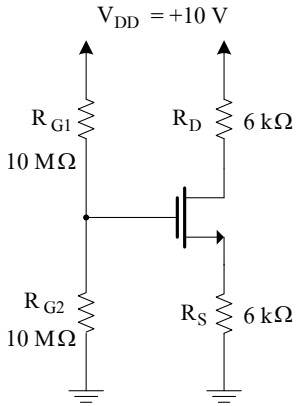
$K_n = k_n'(W/L) = 0.1mA/V^2$



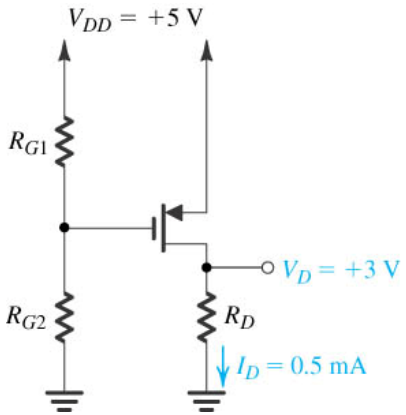
Ex 5.3 Circuit of figure V_D = 0.1 V. The NMOS transistor has V_t = 1 V, $K_n = k_n'(W/L) = 1mA/V^2$



Ex 5.4 find I_D, V_D, V_S and V_{DS}. The NMOS transistor has V_t = 1 V, $K_n = k_n'(W/L) = 0.5mA/V^2$



Ex 5.5 Design the circuit of figure $K_n = k_n'(W/L) = 1mA/V^2$



Example 6.15

In the circuit of Fig. 6.33, determine the region of operation of M_1 as V_1 goes from V_{DD} to zero. Assume $V_{DD} = 2.5$ V and $|V_{TH}| = 0.5$ V.

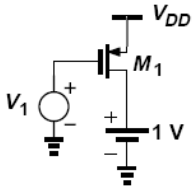


Figure 6.33 Simple PMOS circuit.

Solution

For $V_1 = V_{DD}$, $V_{GS} = 0$ and M_1 is off. As V_1 falls and approaches $V_{DD} - |V_{TH}|$, the gate-source

Ex5.7 Find V_{GS}, I_D and V_{DS} on circuit

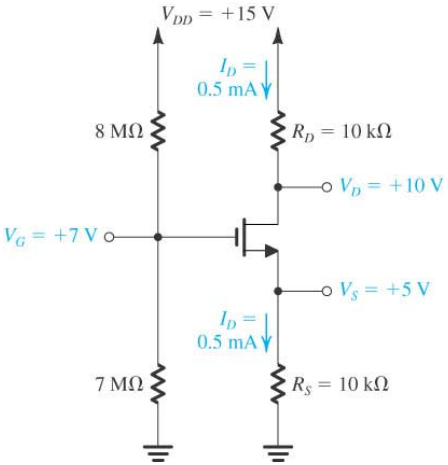


Figure 4.31 Circuit for Example 4.9.

เอกสารอ้างอิง (Reference)

1. Adel S. Sedra, Kenneth C. Smith "Microelectronic Circuit"
2. Pual R. Gray and Robert G. Mayer "Analysis and Design of Integrated Circuit"
3. ผศ.สักรียา ชิตวงศ์ "วิศวกรรมอิเล็กทรอนิกส์"
4. รศ.ดร.ยุ ทธนา กุ ลวิ ทิ ต"เอกสารประกอบการสอน วิ ชาวงจรอิ เล็ กทรอนิ กส์ "

Thank you