มหาวิทยาลัยราชภัฏนครปฐม
Nakhon Pathom Rajabhat University

Lecture 5 Differential and Multistage Amplifiers

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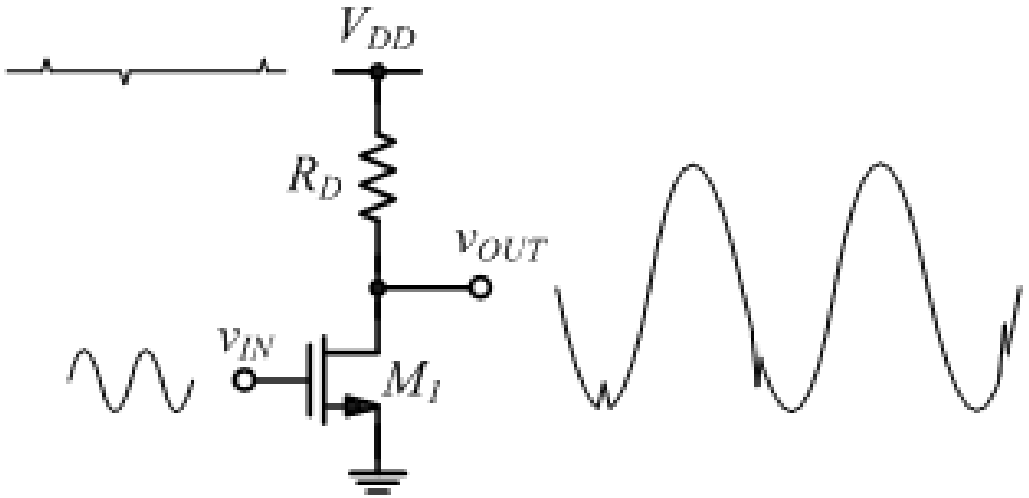
มหาวิทยาลัย
ราชภัฏนครปฐม

Outline

- The BJT Differential Pair
- Small Signal Operation of The BJT Differential Amplifier
- Other Nonideal Differential Amplifier
- Biasing in BJT Integrated Circuit
- BJT Differential Amplifier
- MOS Differential Amplifiers
- Multistage Amplifiers

5.1 Introduction



5.1 Introduction

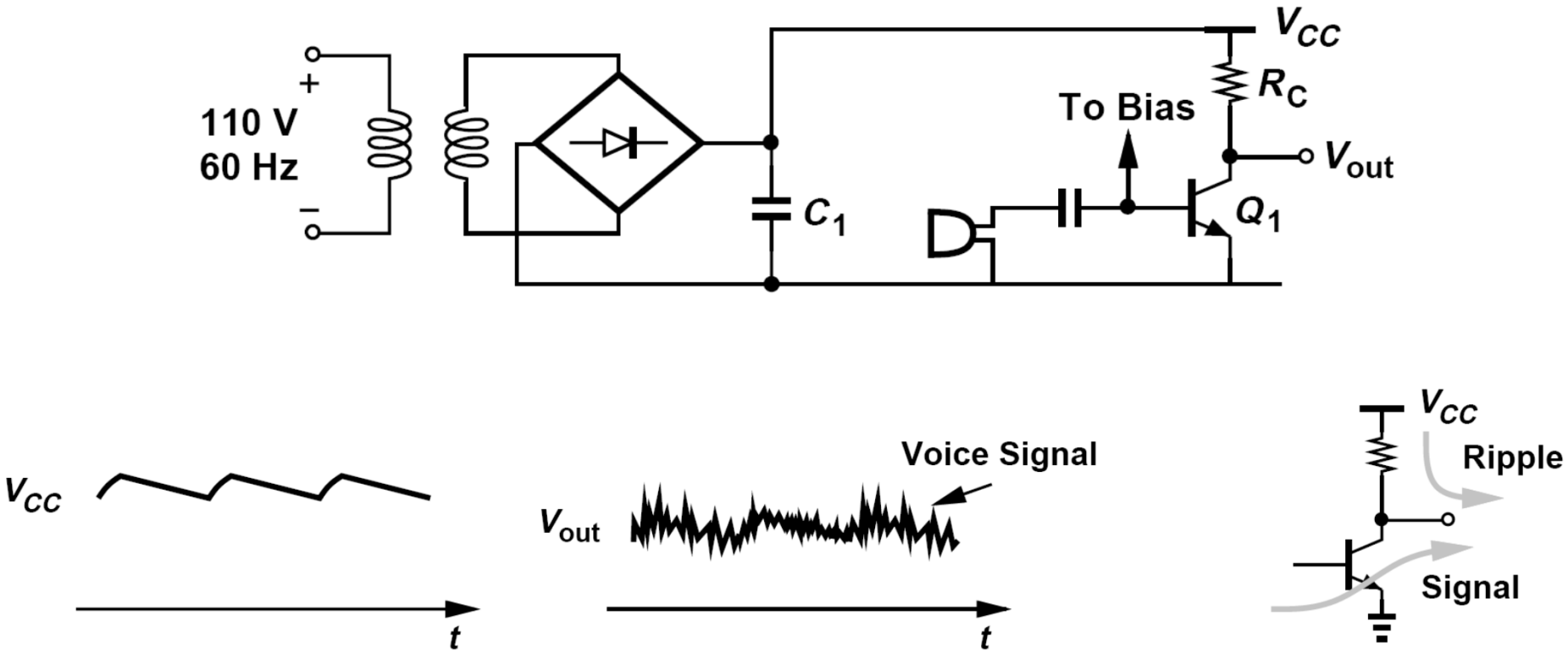
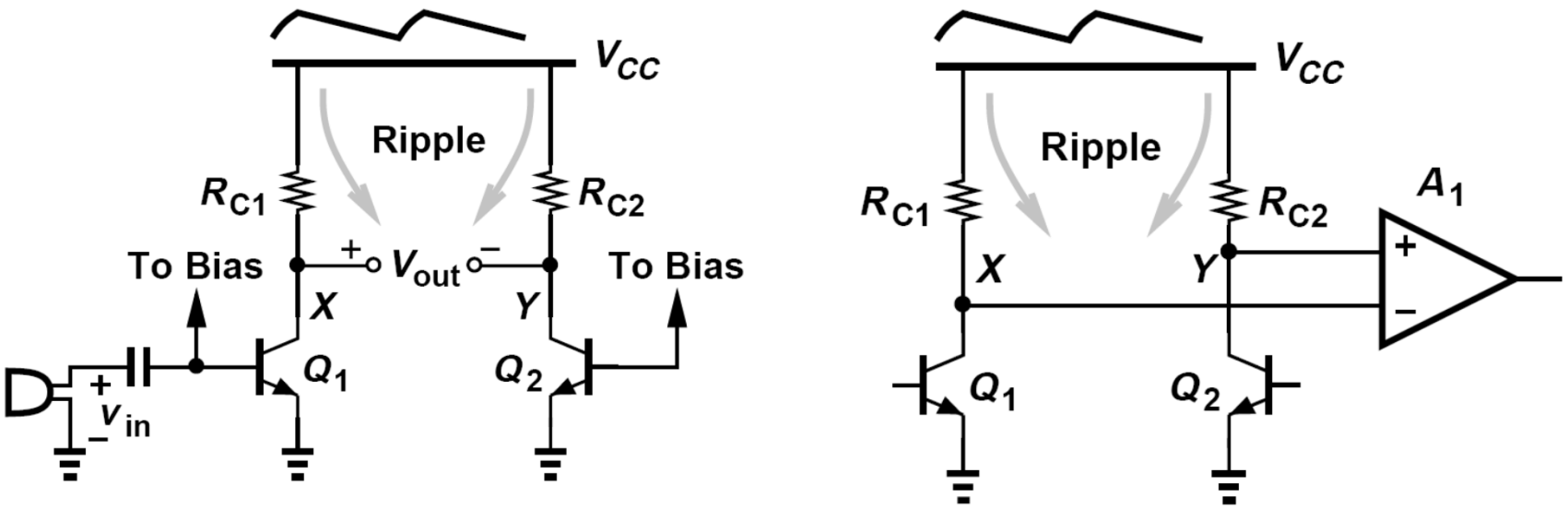


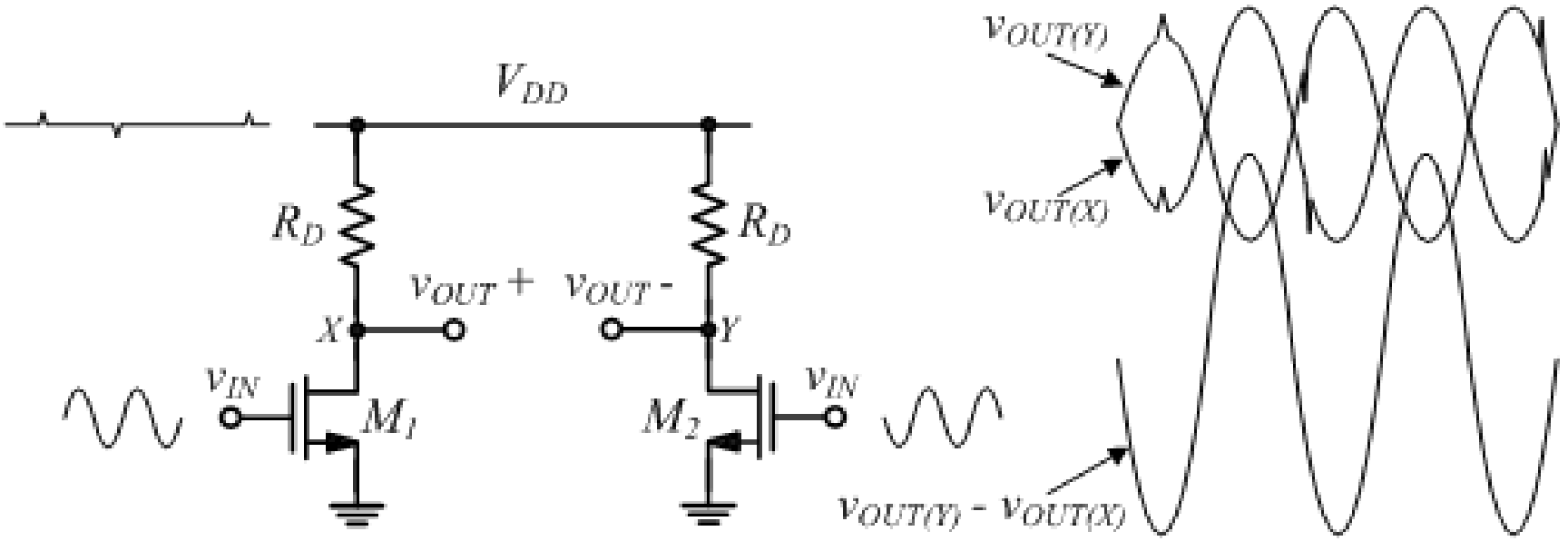
Figure 10.1 (a) CE stage powered by a rectifier, (b) ripple on supply voltage, (c) effect at output, (d) ripple and signal paths to output.

5.1 Introduction

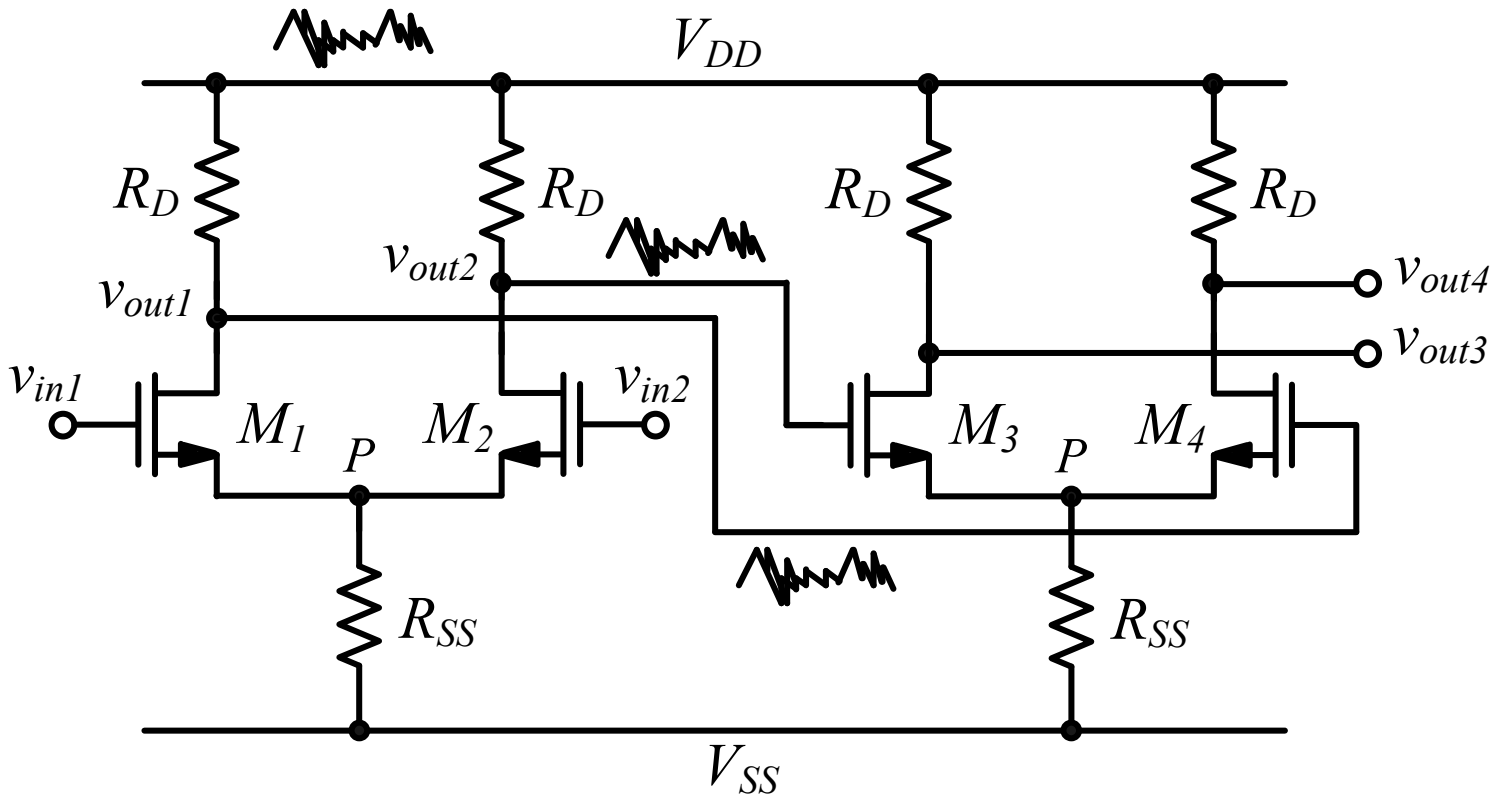


รูปที่ 5.2 การใช้วงจรขยาย CE สองภาคเพื่อกำจัดผลกระทบของริปเปิล

5.1 Introduction



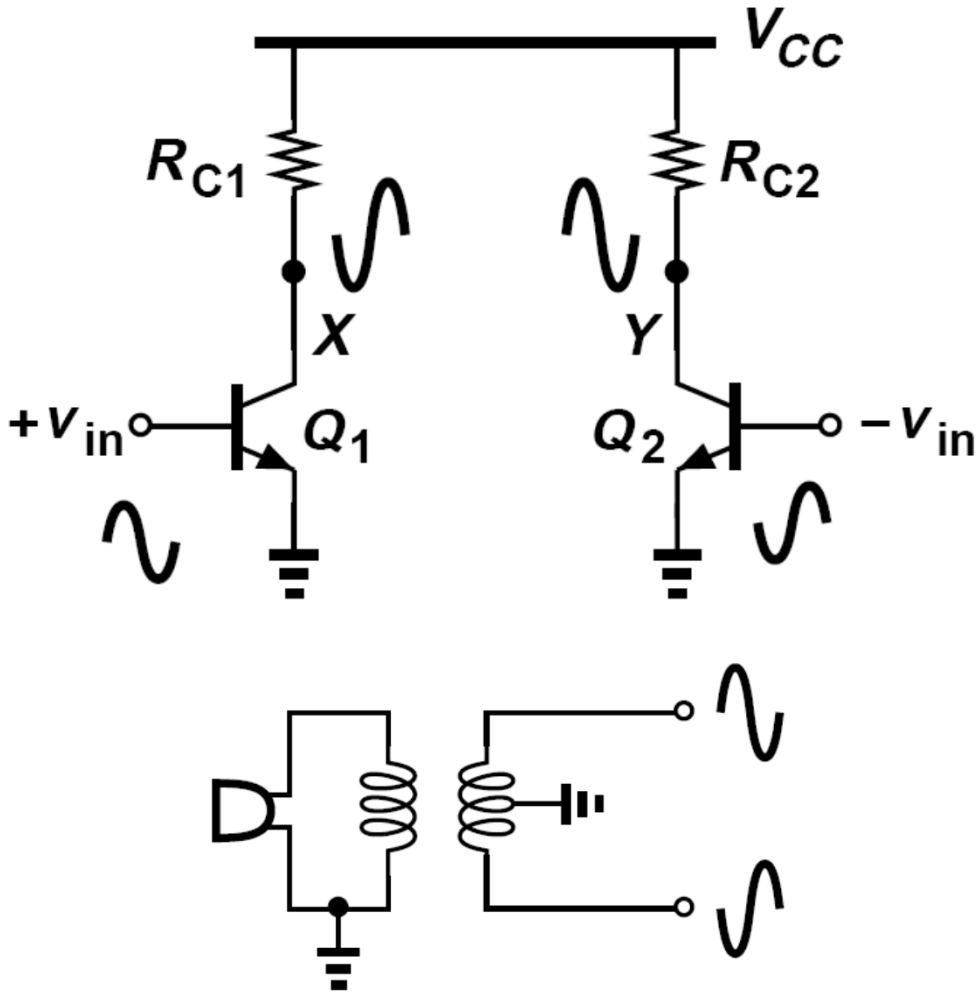
5.1 Introduction

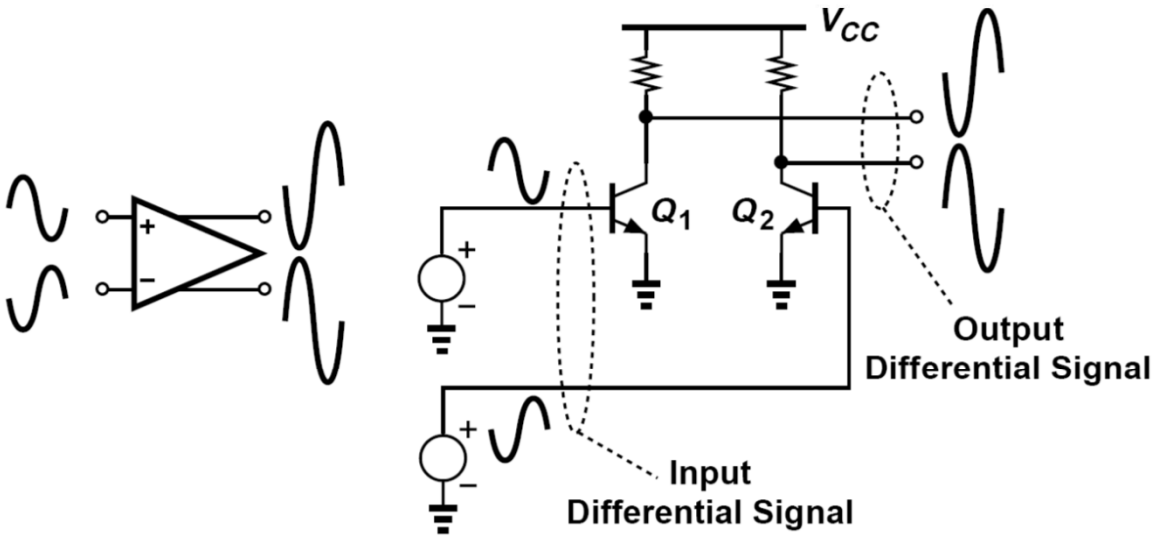


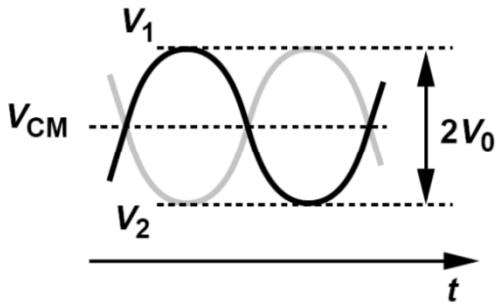
5.2 Signal

- สัญญาณโหมดผลต่าง (Differential mode signal) คือ ระดับของสัญญาณที่วงจรที่มีค่าแตกต่างกัน
- สัญญาณโหมดร่วม (Common mode signal) คือ ระดับของสัญญาณที่วงจรใช้ร่วมกัน

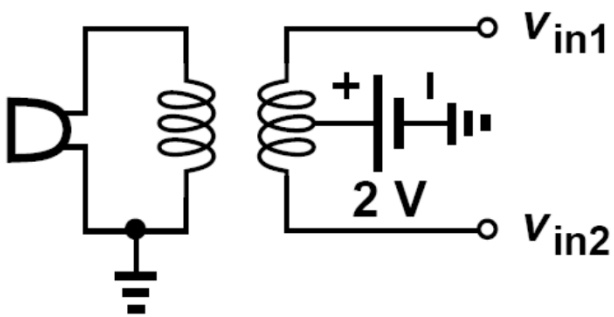
5.2 Differential Mode Signals

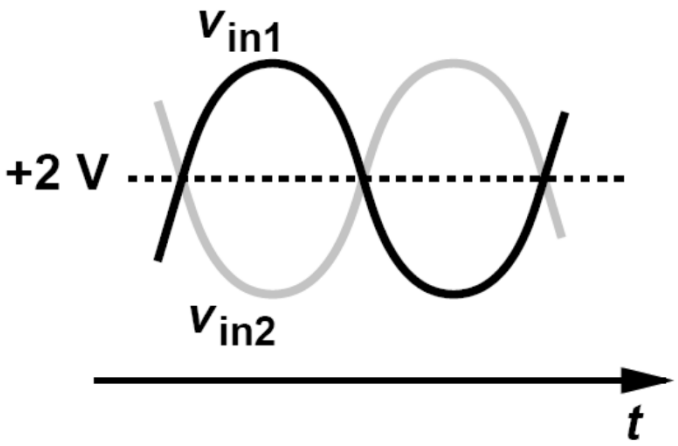



V_{CC}
Q_1
Q_2
Output
Differential Signal
Input
Differential Signal

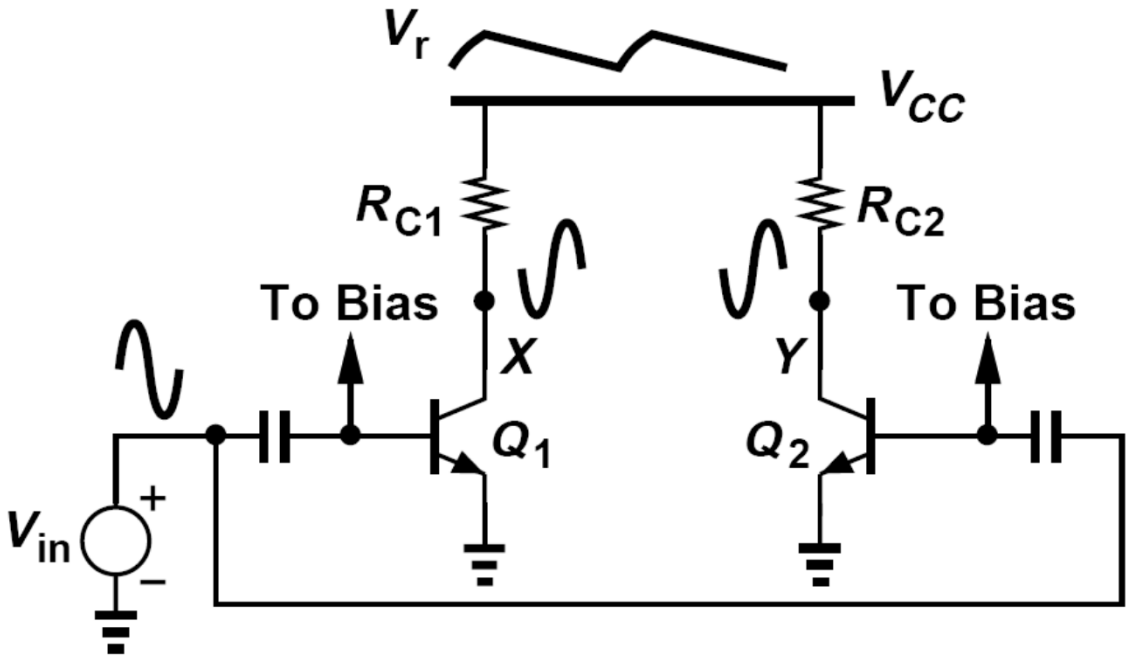

V_1
V_{CM}
$2V_0$
V_2
t

5.3 Common Mode Signals

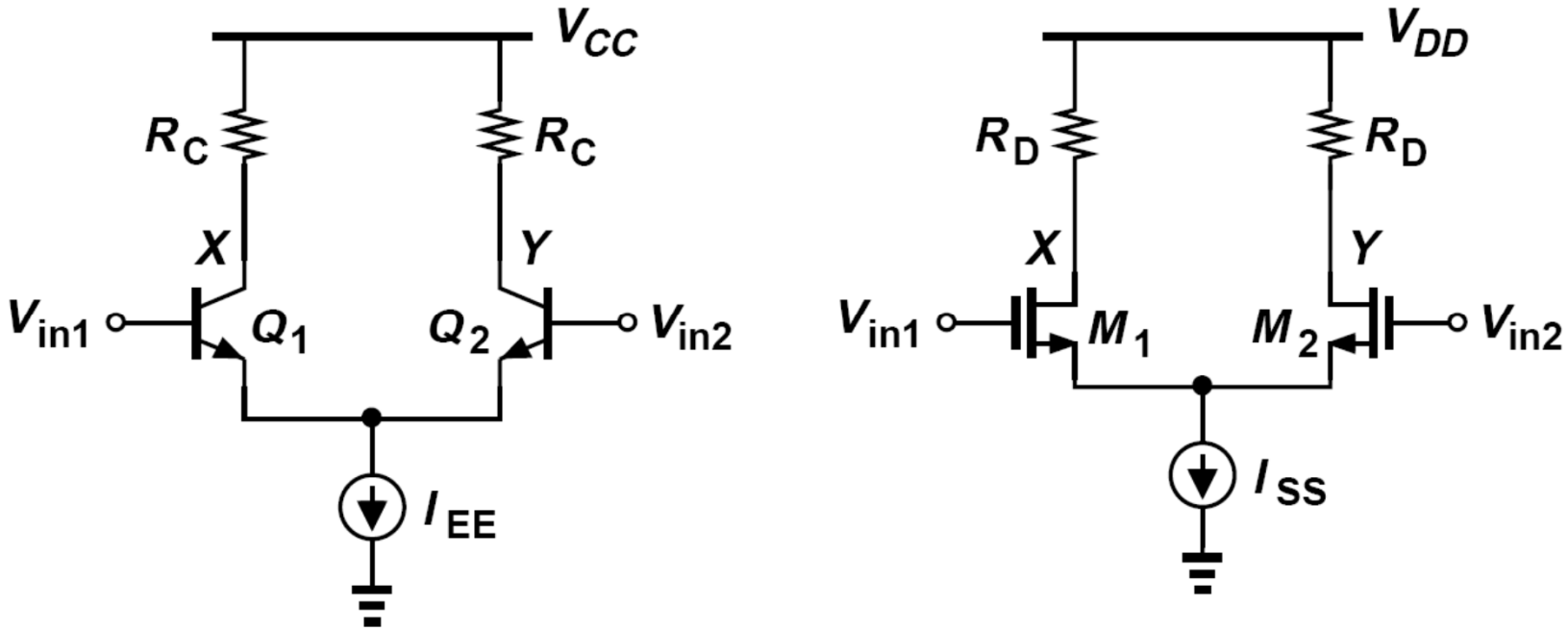




5.3 Common Mode Signals

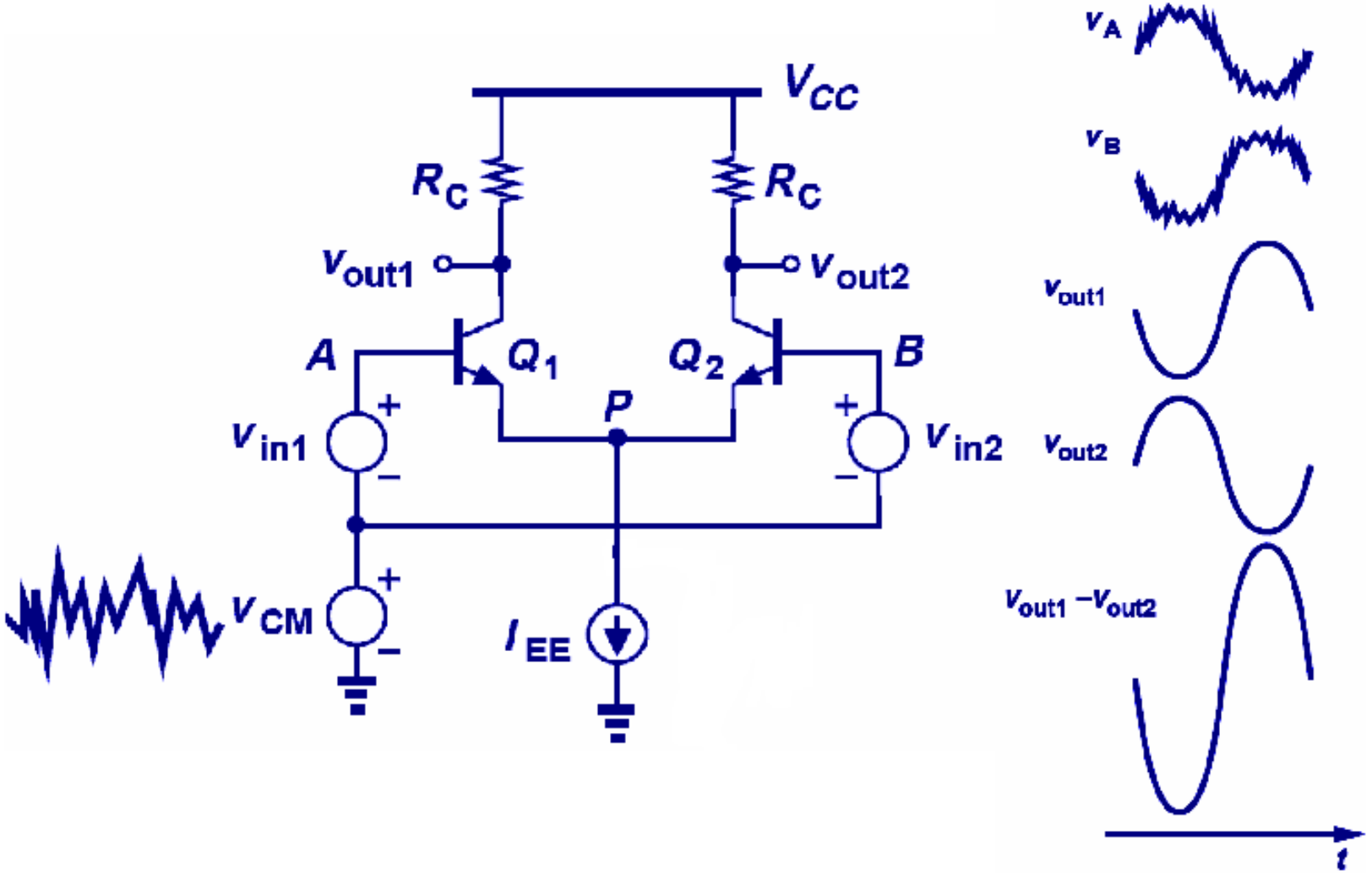


5.4 Differential pair

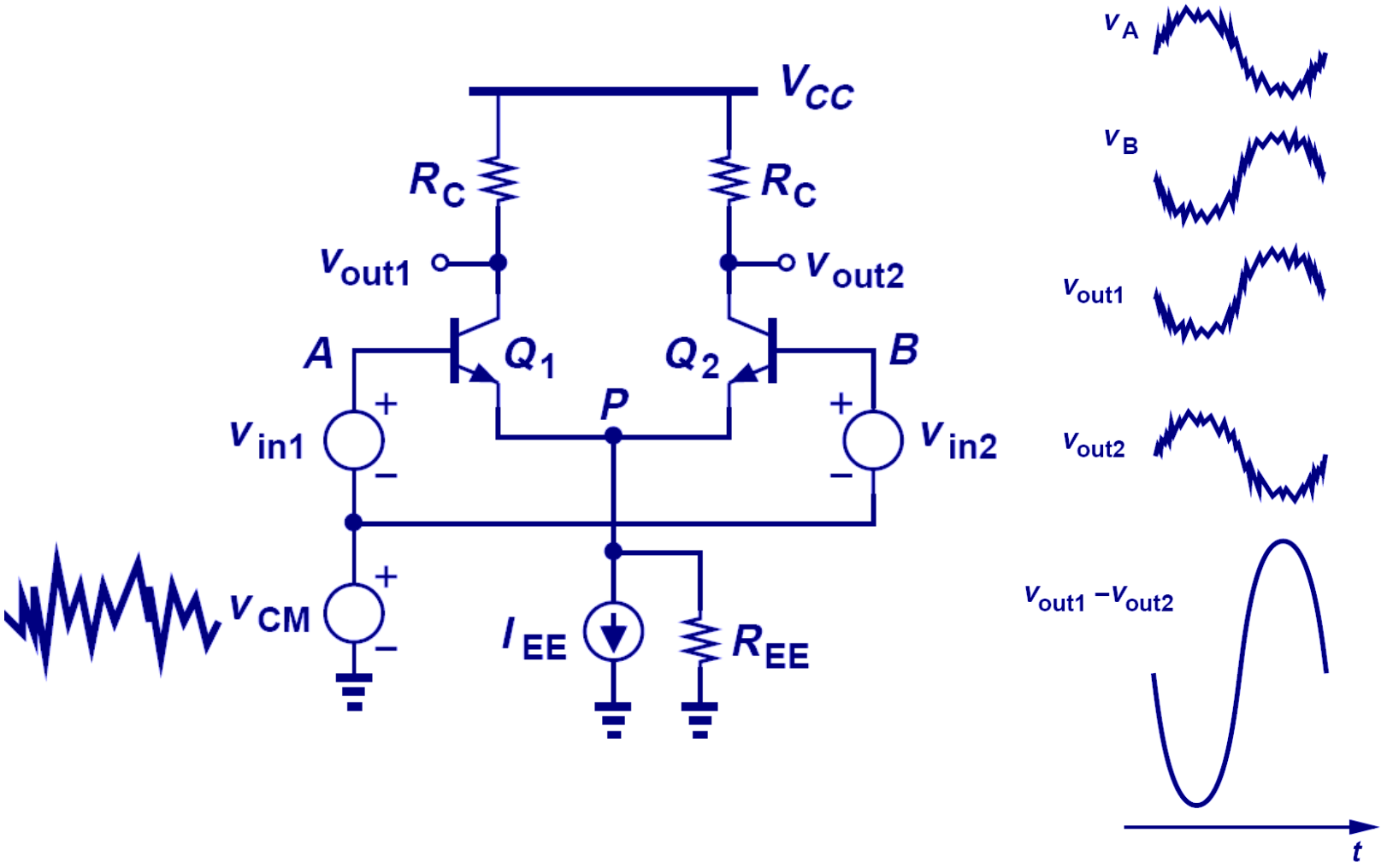


รูปที่ 5.6 วงจรขยายคู่ผลต่าง (ก) ไบโพล่า (ข) มอสเฟต

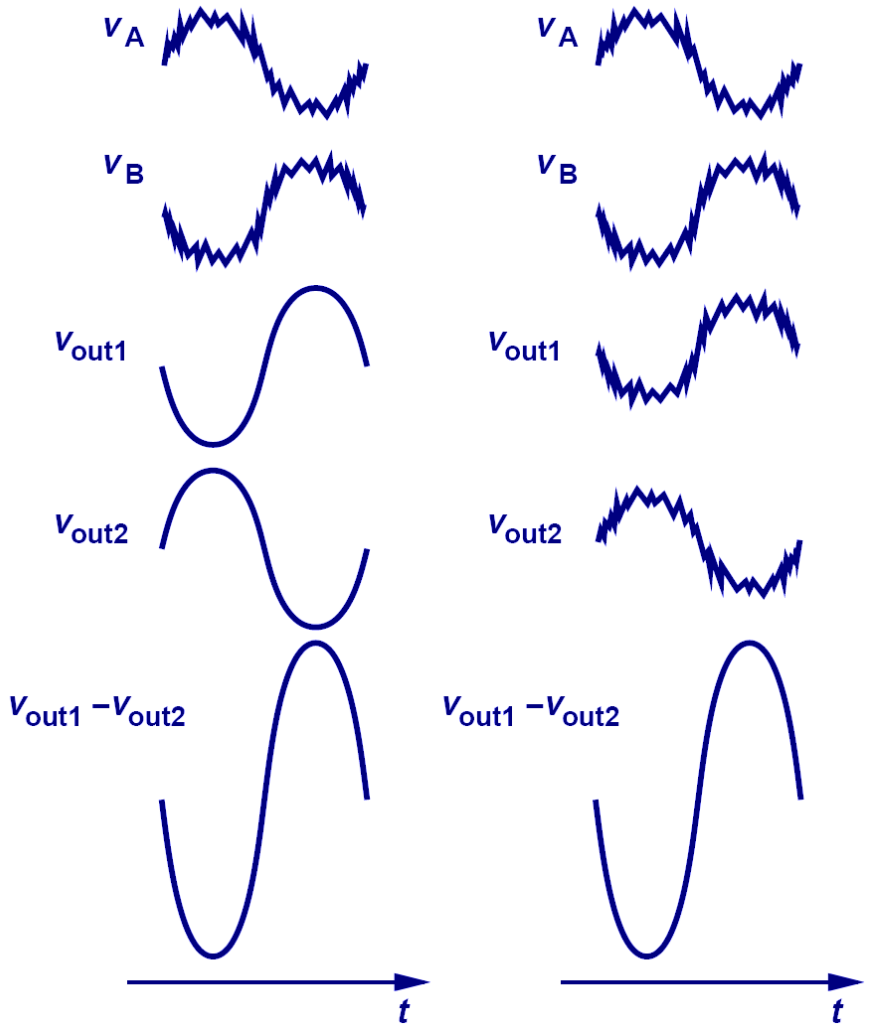
5.5 Input CM Noise with Ideal Tail Current



5.6 Input CM Noise with Non-ideal Tail Current



5.7 Comparison



- As it can be seen, the differential output voltages for both cases are the same. So for small input CM noise, the differential pair is not affected.

MOSFET Differential Amplifier.

- Signal analysis of differential amplifier
  - differential mode signal analysis
  - common mode signal analysis

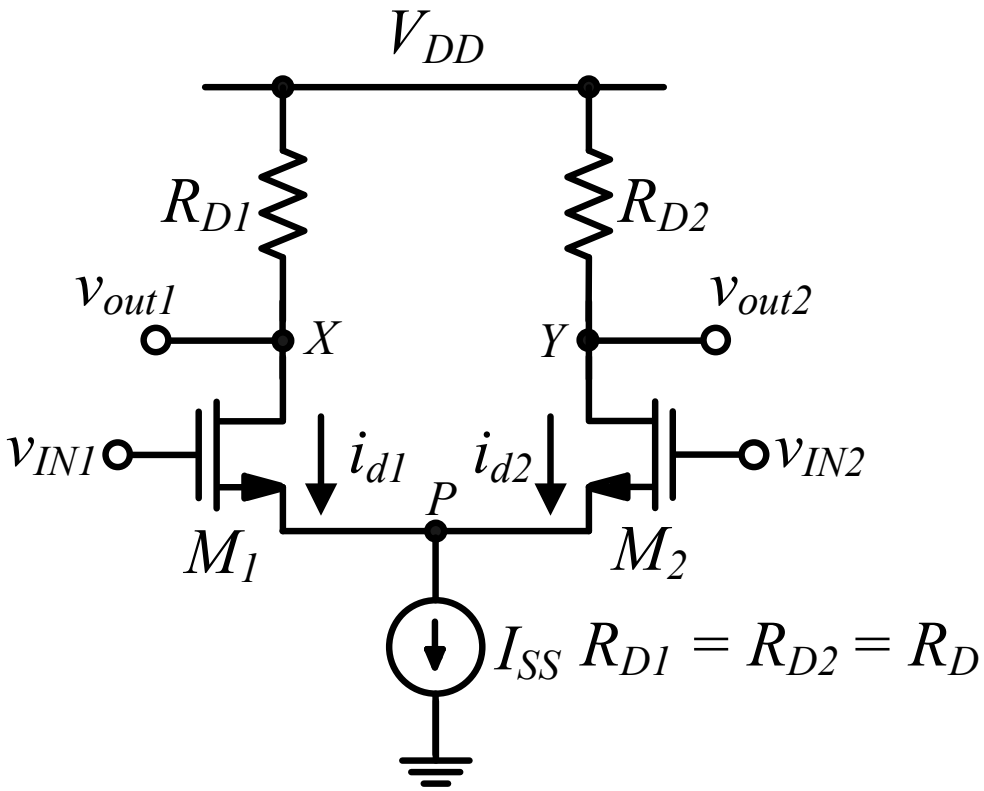
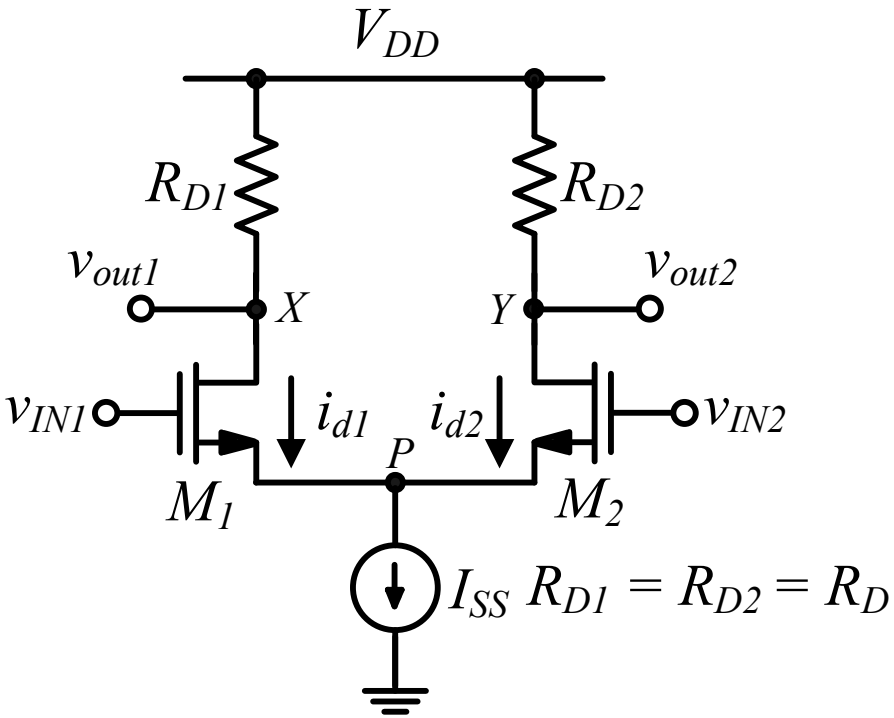
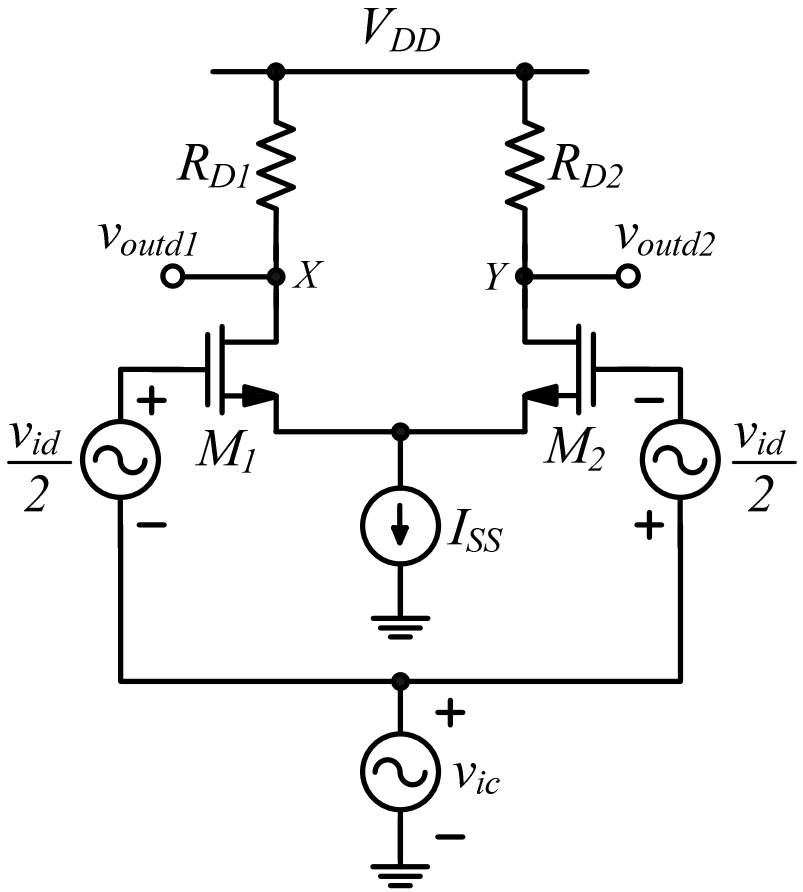


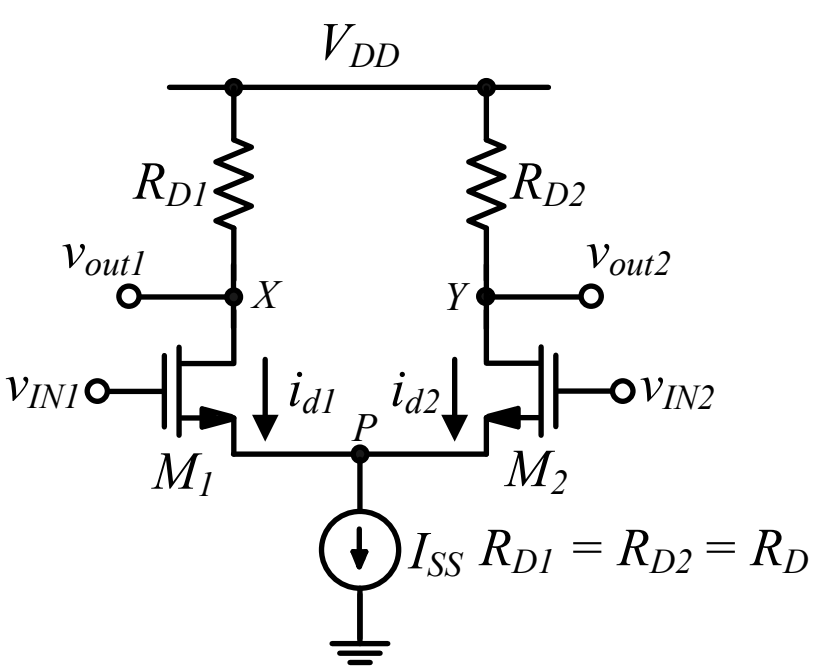
Fig 5.12 The basic MOS differential-pair configuration.

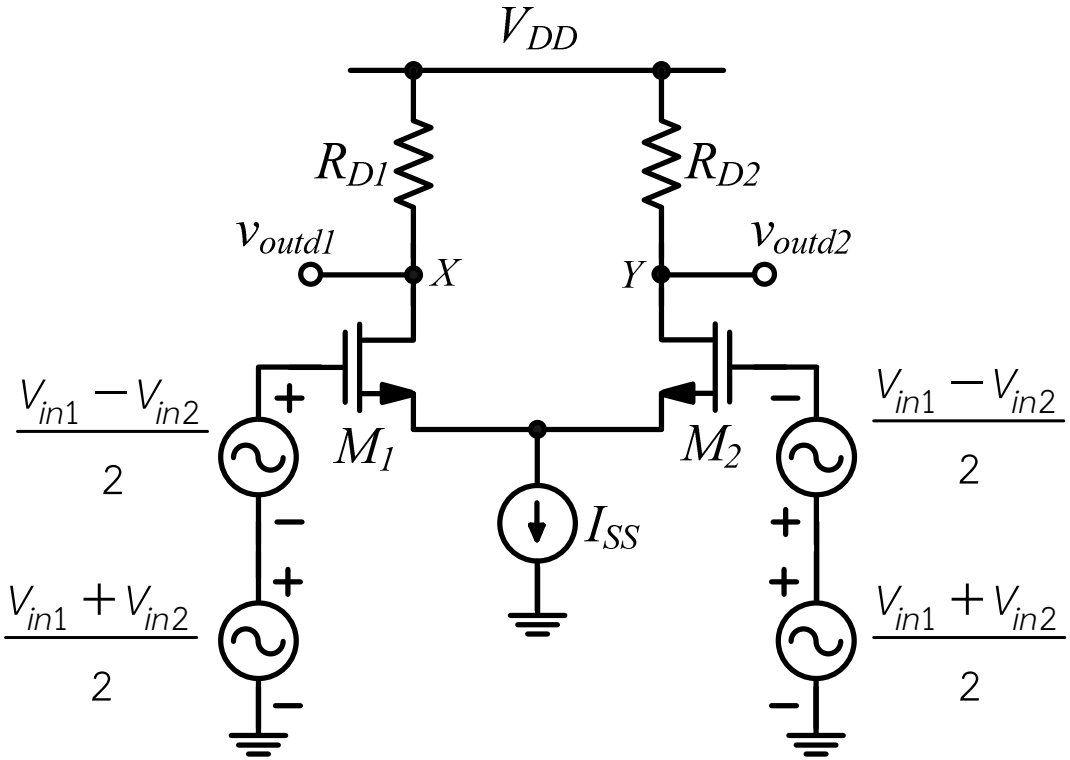

V_{DD}
R_{D1}
R_{D2}
v_{out1}
v_{out2}
X
Y
v_{IN1}
v_{IN2}
i_{d1}
i_{d2}
P
M_1
M_2
I_{SS}

$R_{D1} = R_{D2} = R_D$

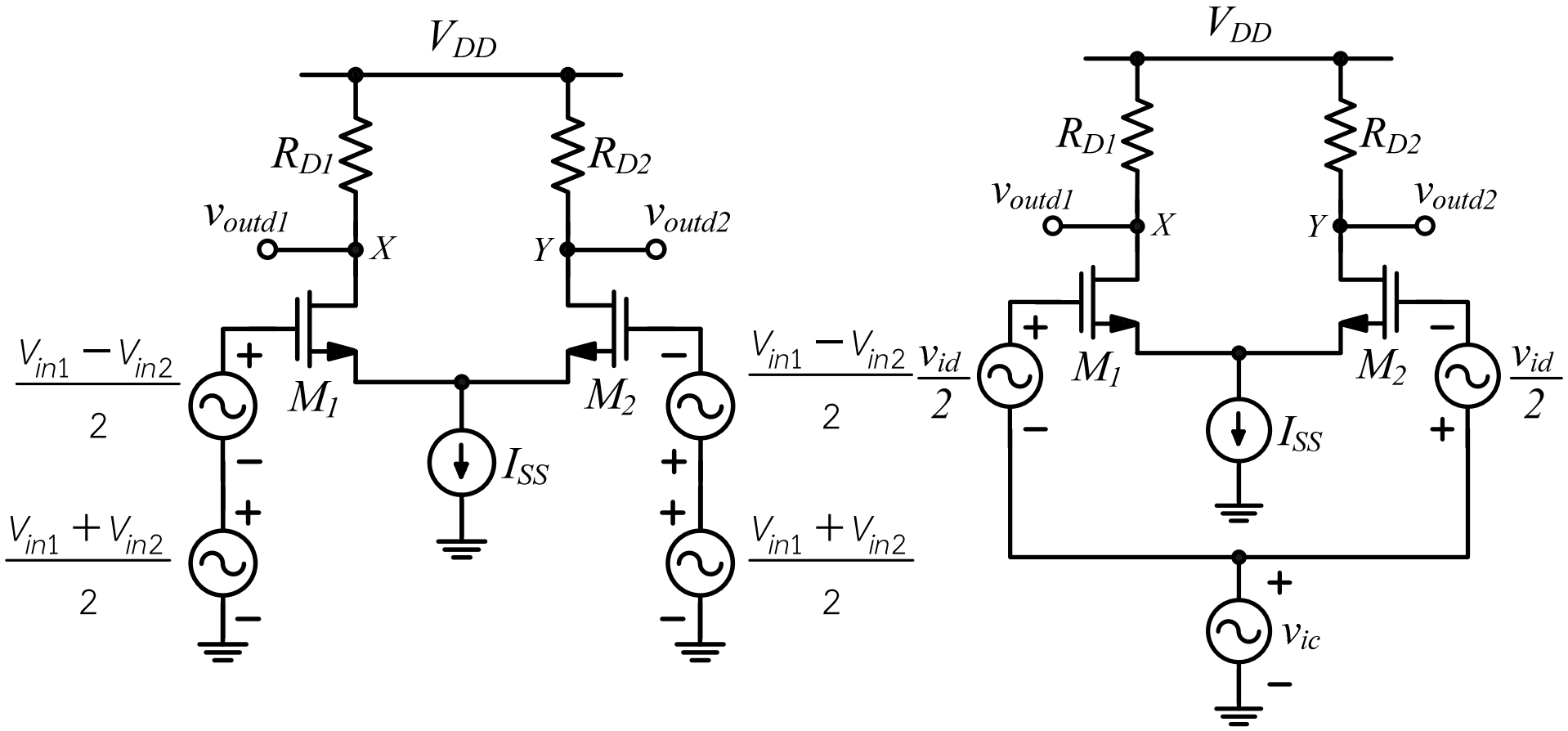

V_{DD}
R_{D1}
R_{D2}
v_{outd1}
v_{outd2}
X
Y
$\frac{v_{id}}{2}$
M_1
M_2
I_{SS}
v_{ic}

Differential Response

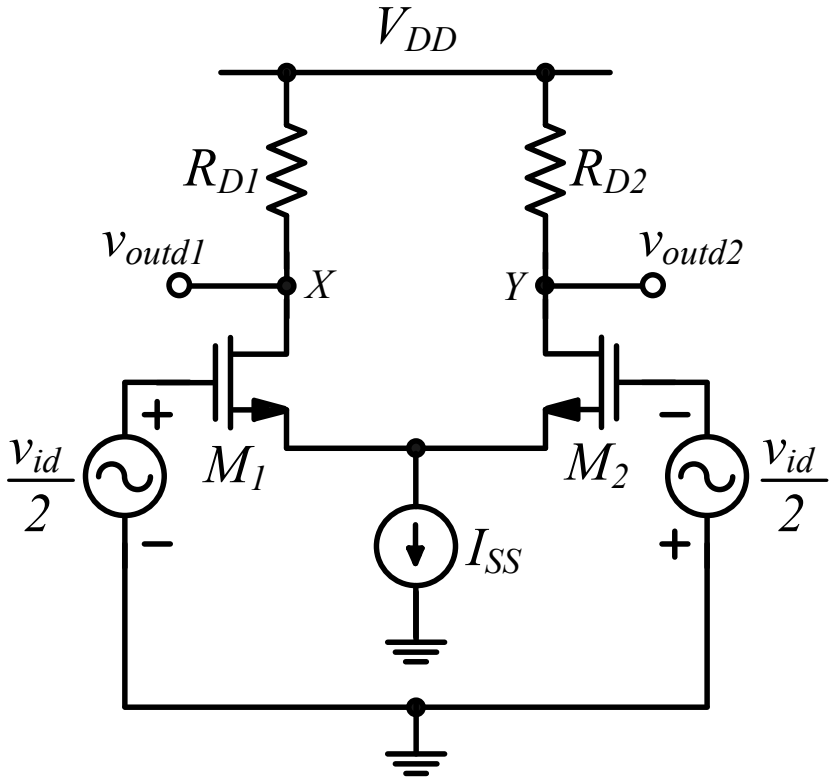


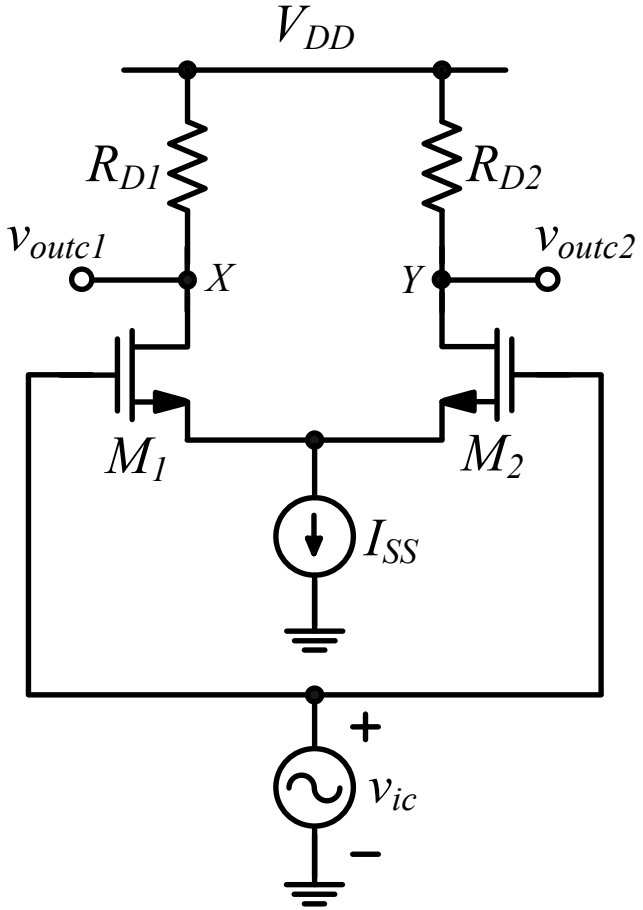


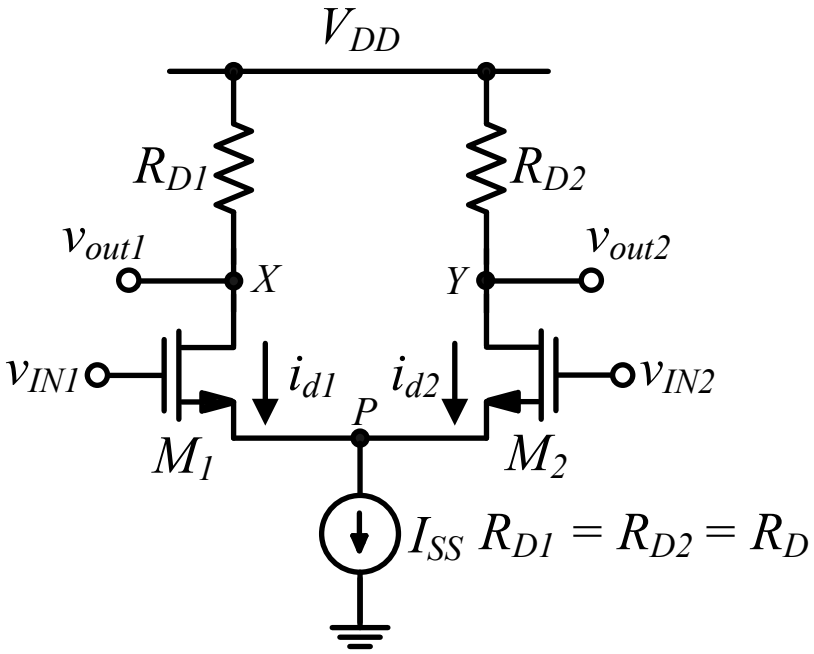
Differential Response

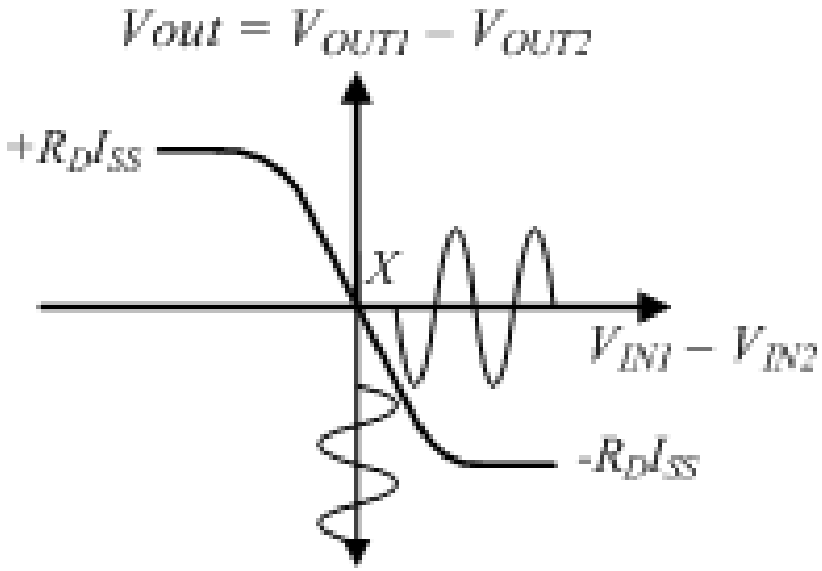


Differential Response

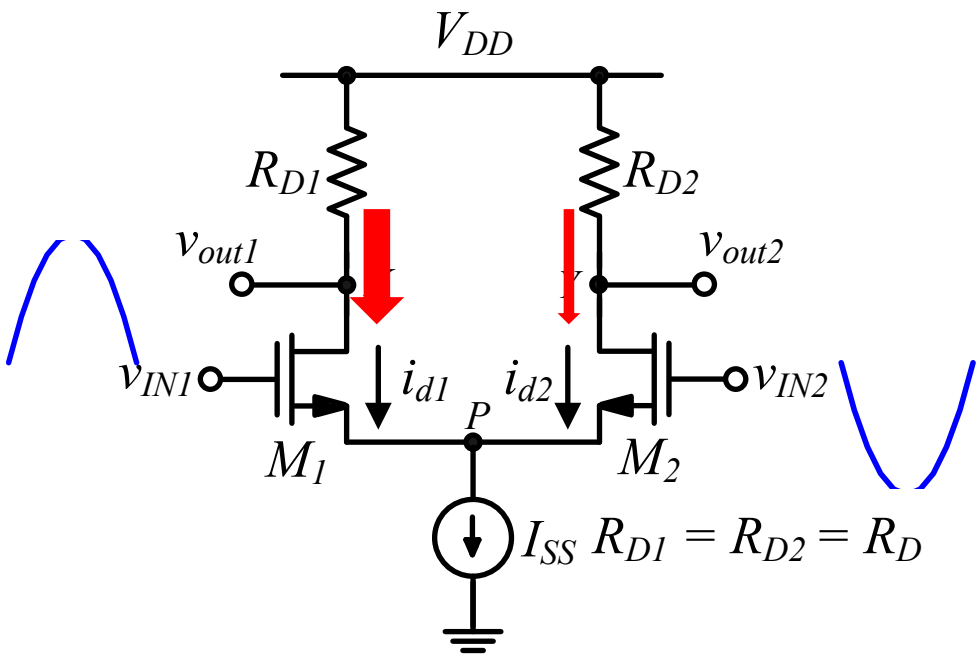


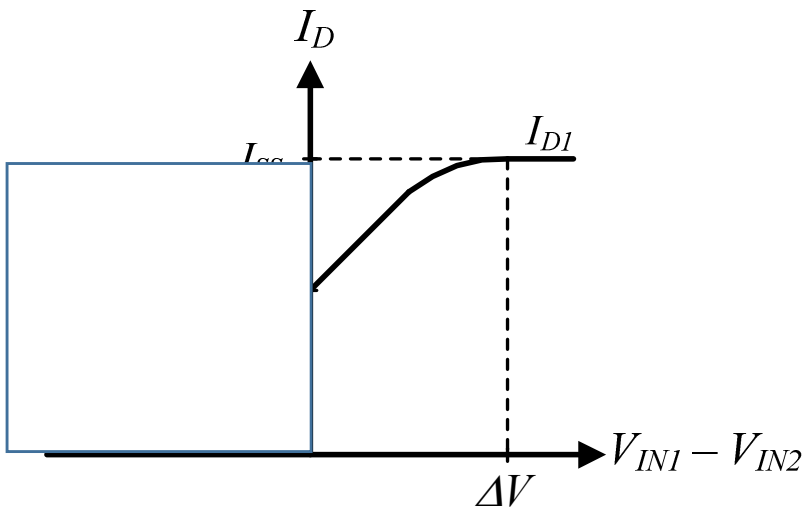


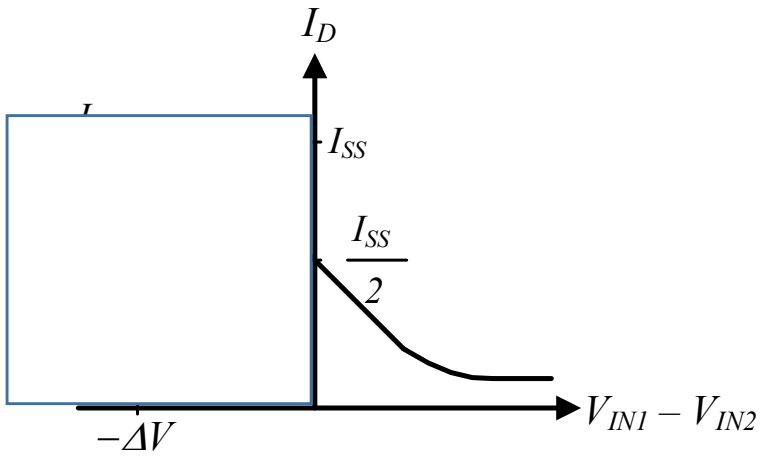

V_{DD}
R_{D1}
R_{D2}
v_{out1}
v_{out2}
X
Y
v_{IN1}
v_{IN2}
i_{d1}
i_{d2}
P
M_1
M_2
I_{SS} $R_{D1} = R_{D2} = R_D$


$V_{out} = V_{OUT1} - V_{OUT2}$
$+R_D I_{SS}$
X
$V_{IN1} - V_{IN2}$
$-R_D I_{SS}$

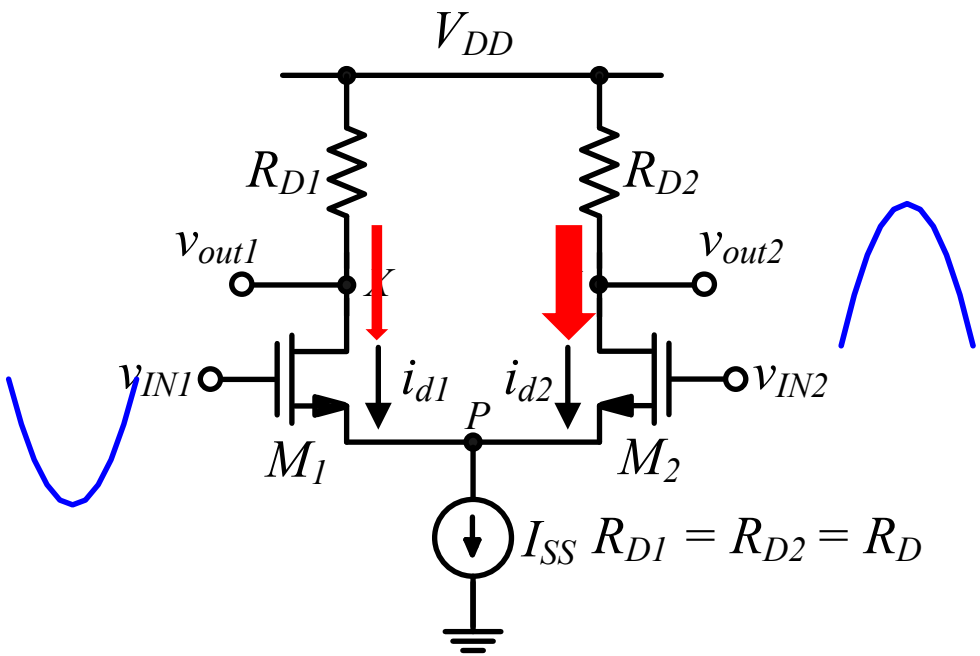
Differential Response

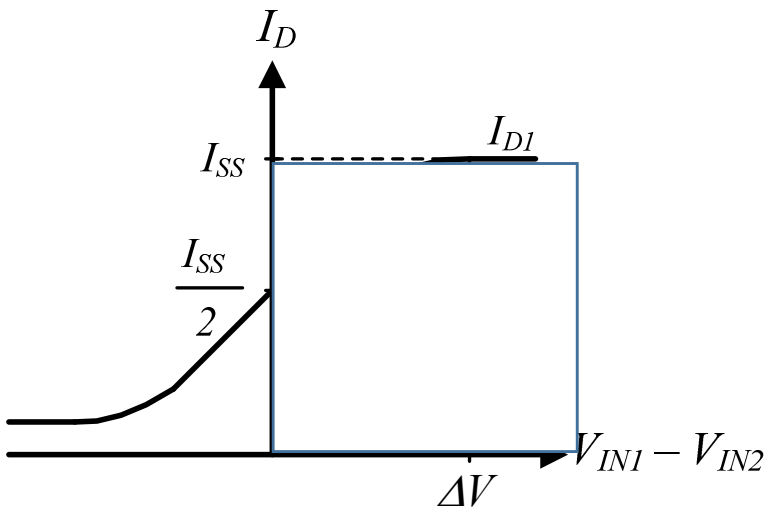


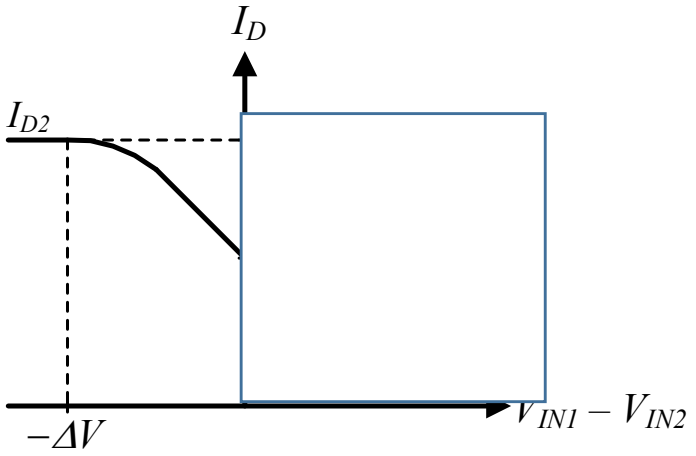




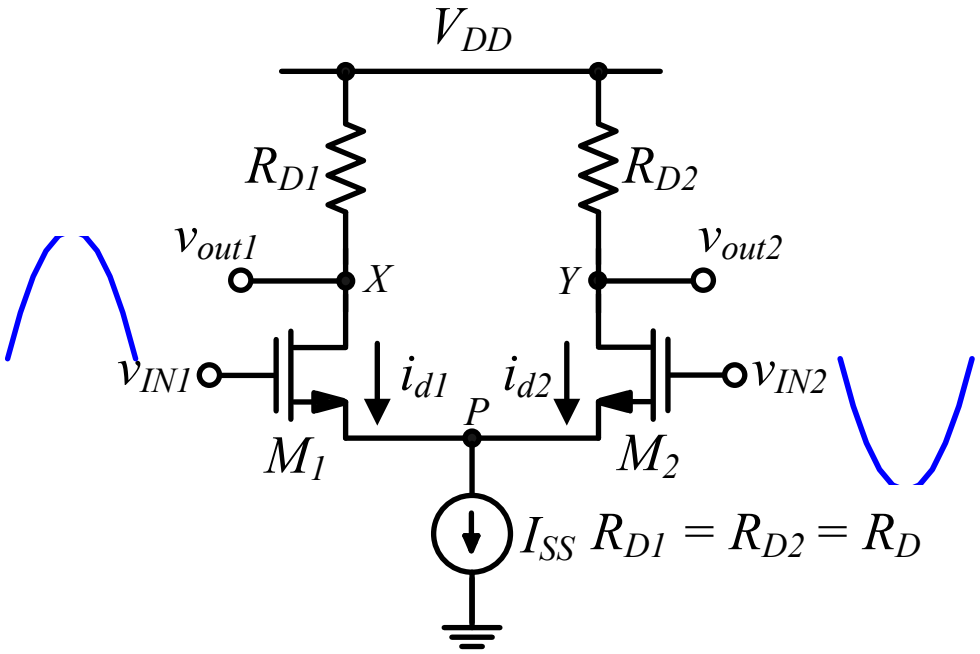
Differential Response

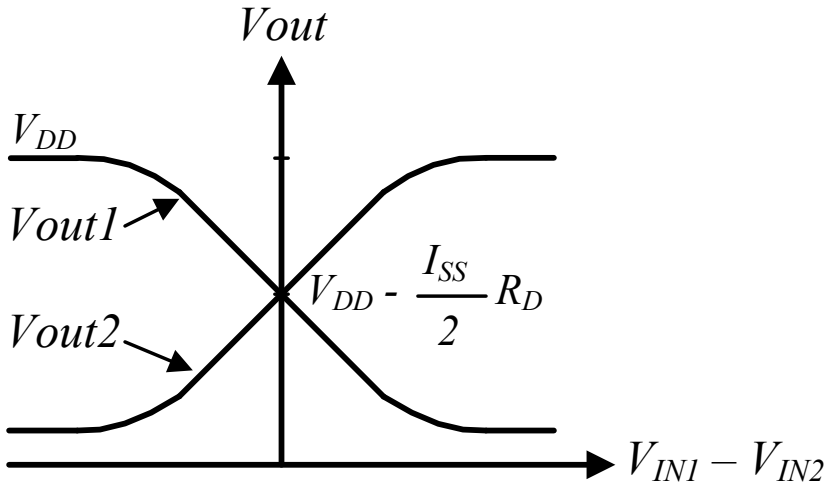




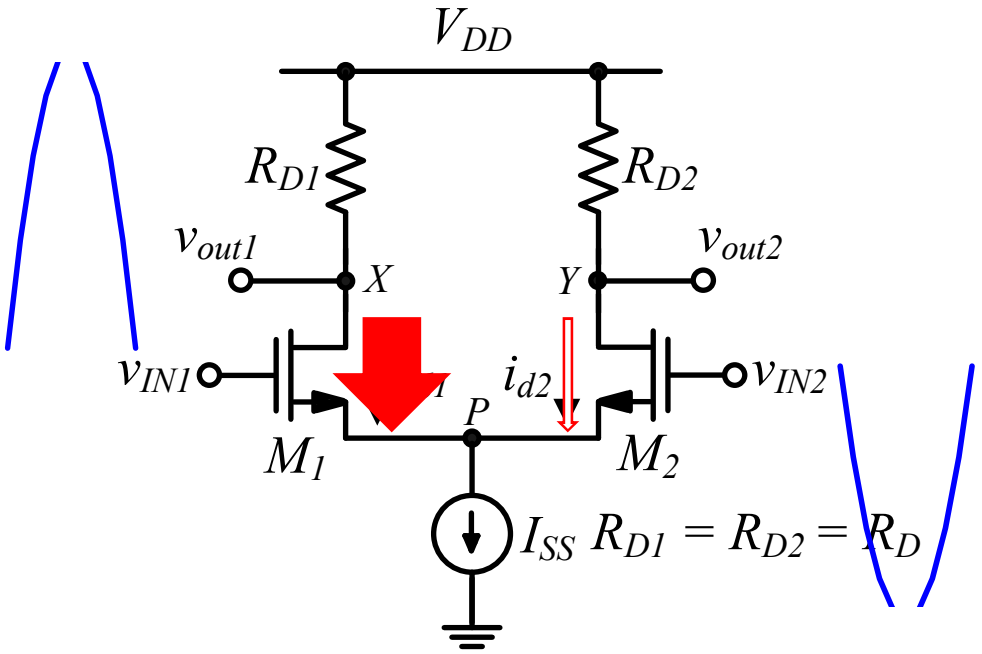


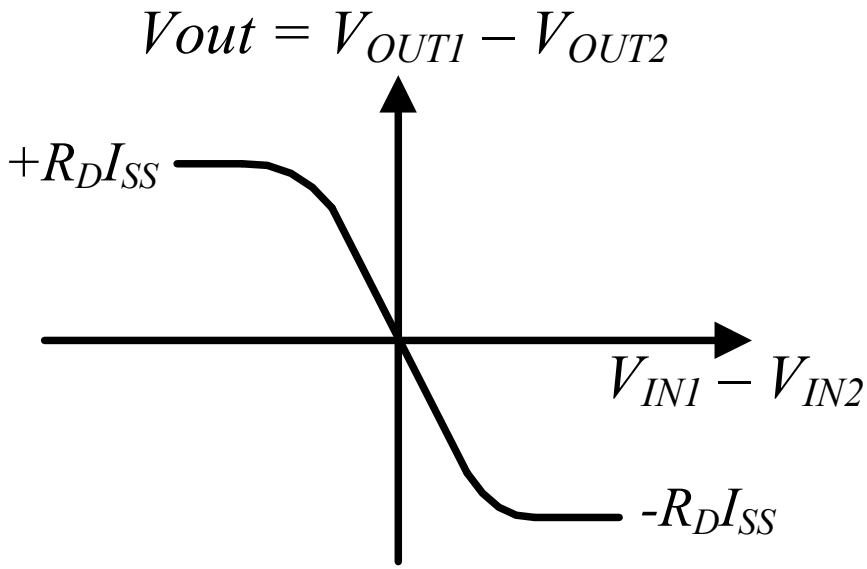
Differential Response



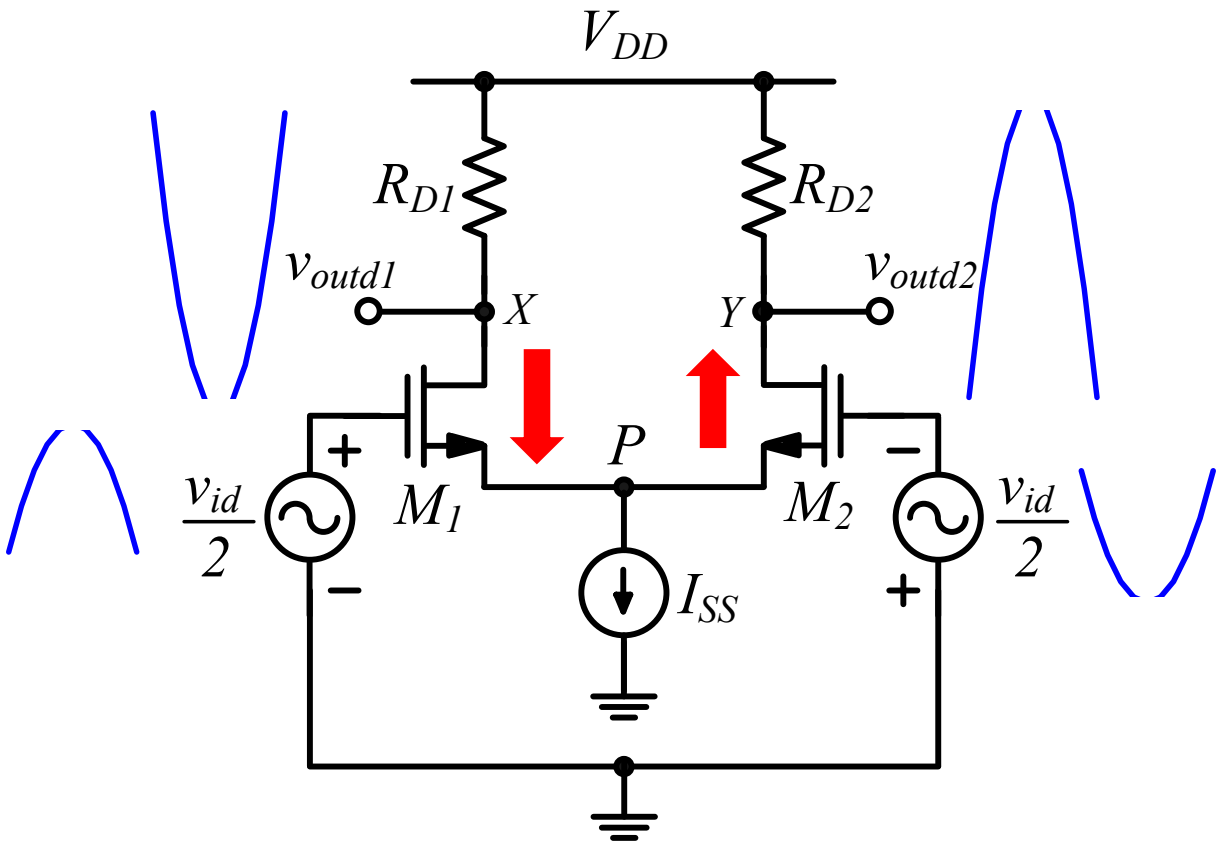


Differential Response

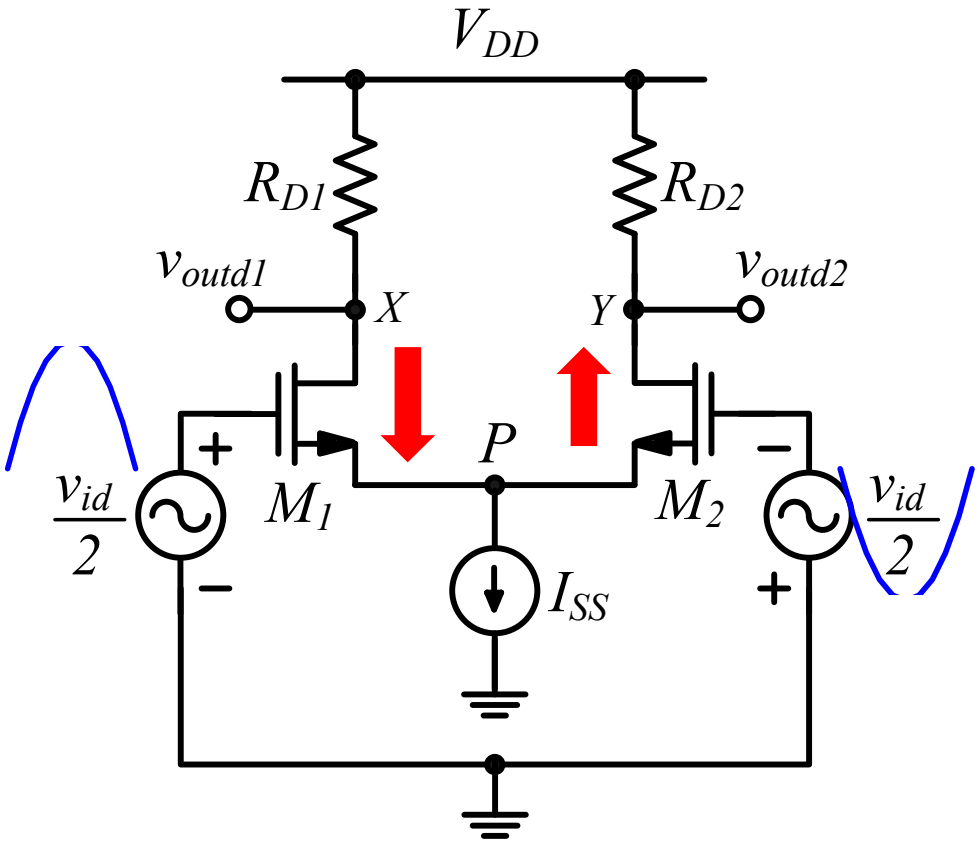


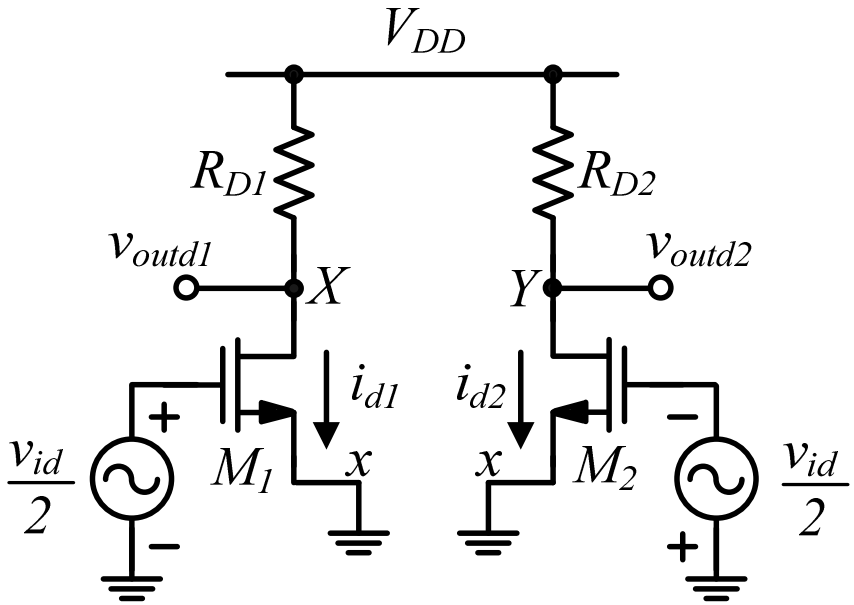


Differential Response

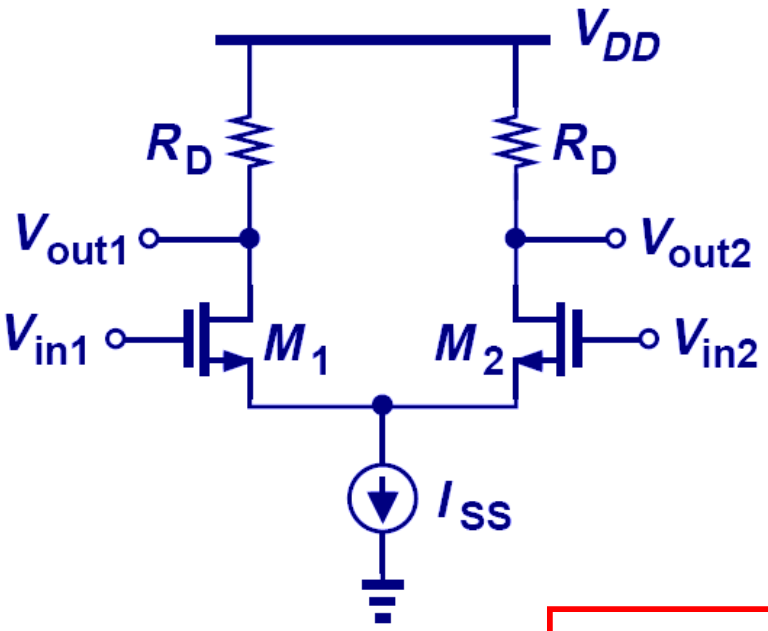


Differential Response





MOS Differential Pair's Large-Signal Response

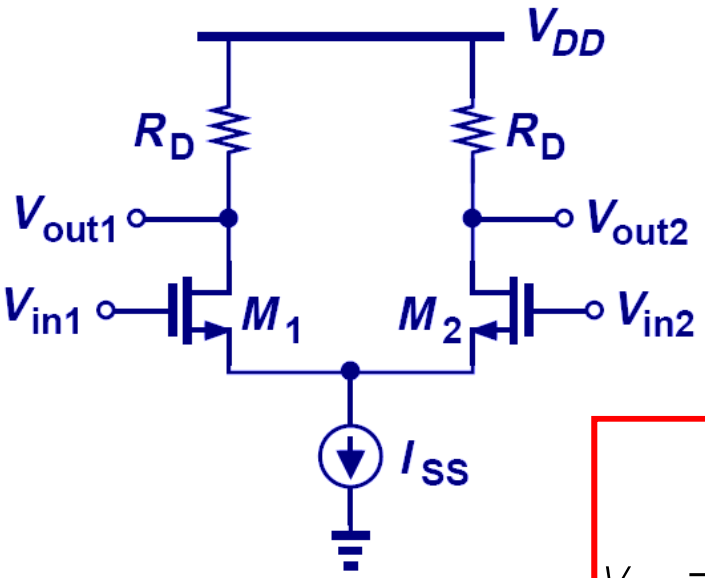


$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$V_{in1} - V_{in2} = \left(\sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} + V_{TH} \right) - \left(\sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} + V_{TH} \right)$$

$$I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{in1} - V_{in2} \right) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - \left(V_{in1} - V_{in2} \right)^2}$$

MOS Differential Pair's Small-Signal Response



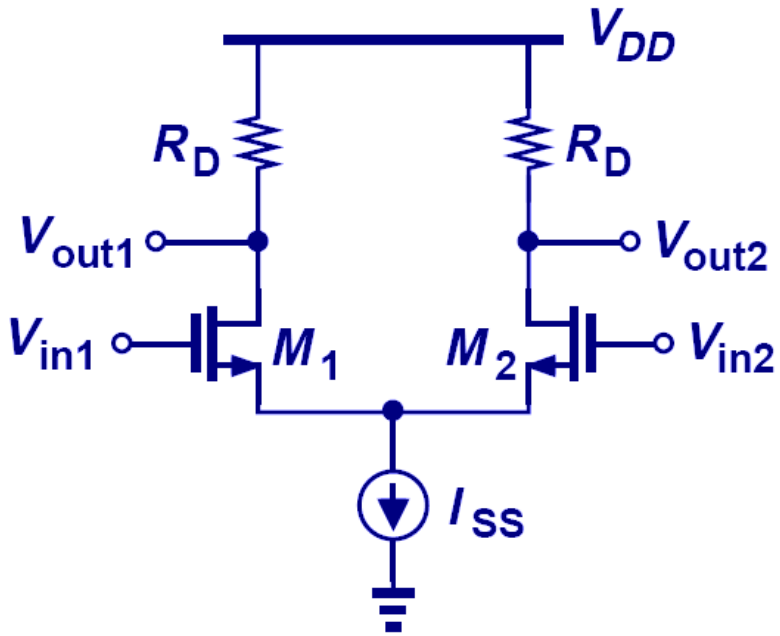
$$V_{out} = V_{out1} - V_{out2} = -(I_{D1} - I_{D2})R_D$$

$$V_{out1} = V_{DD} - I_{D1}R_D \qquad V_{out2} = V_{DD} - I_{D2}R_D$$

$$V_{out} = V_{out1} - V_{out2} = -(I_{D1} - I_{D2})R_D$$

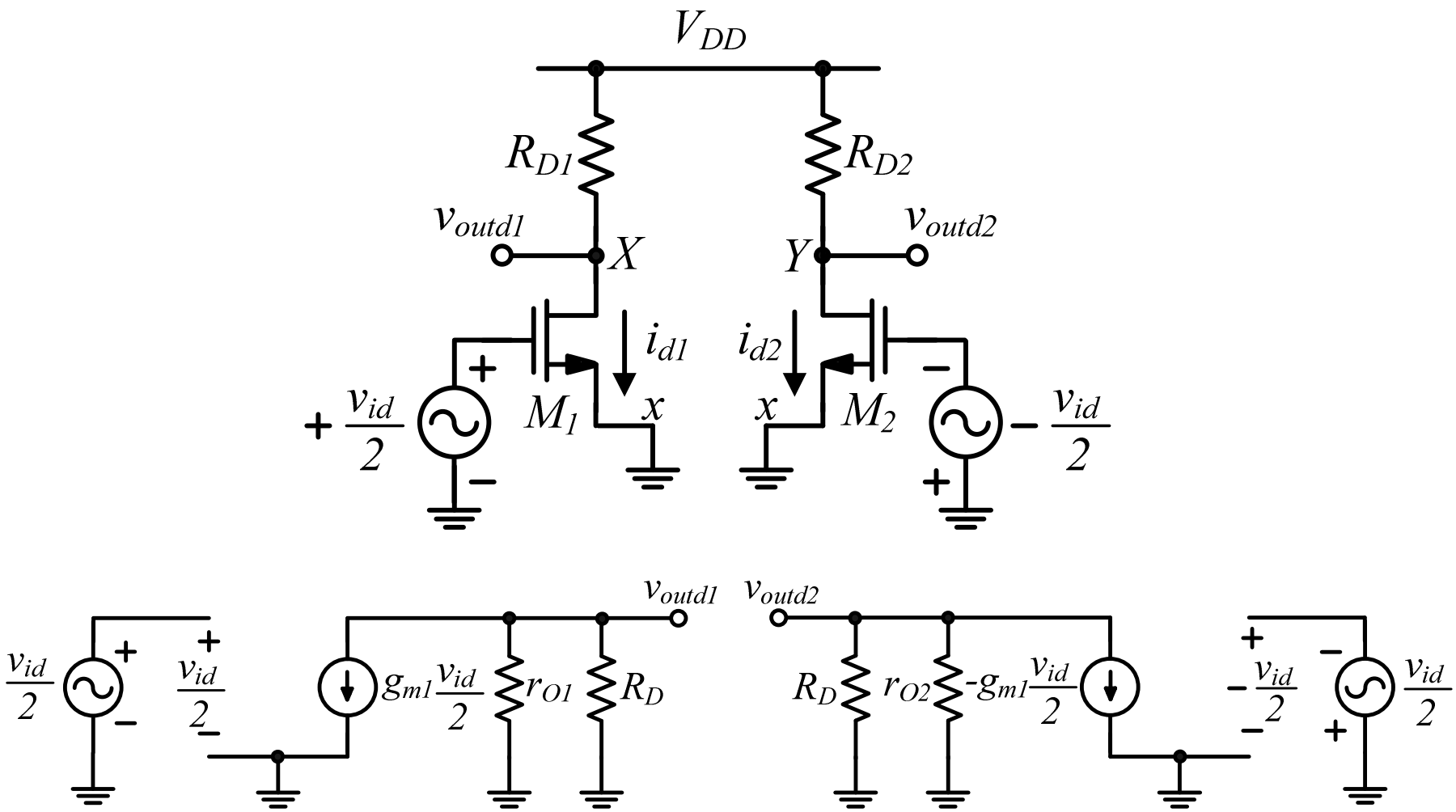
$$V_{out} = -\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in1} - V_{in2}\right)\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \left(V_{in1} - V_{in2}\right)^2}\right]R_D$$

MOS Differential Pair's Large-Signal Response



$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in1} - V_{in2}\right)\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \left(V_{in1} - V_{in2}\right)^2}$$

Differential Response



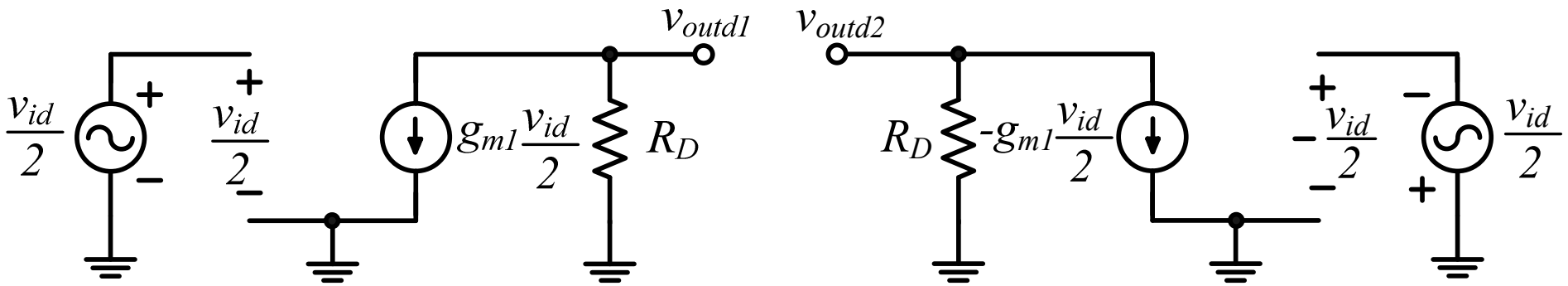
A_{vd} and A_{vc}

$$A_{vd} = \left.\frac{V_{outd}}{V_{id}}\right|_{V_{ic}=0}$$

$$A_{vc} = \left.\frac{V_{outc1,2}}{V_{ic}}\right|_{V_{id}=0}$$

$$V_{outd} = V_{outd1} - V_{outd2} = A_{vd}V_{id}$$

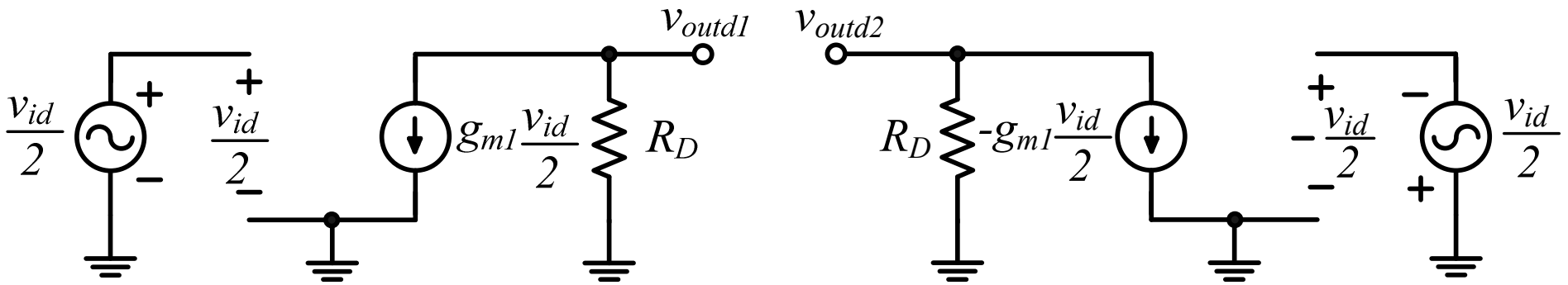
Small-Signal Analysis of MOS Differential Pair



$$V_{outd1} = -g_{m1}R_D\frac{V_{id}}{2}$$

$$V_{outd2} = -g_{m2}R_D\left(-\frac{V_{id}}{2}\right)$$

Virtual Ground and Half Circuit

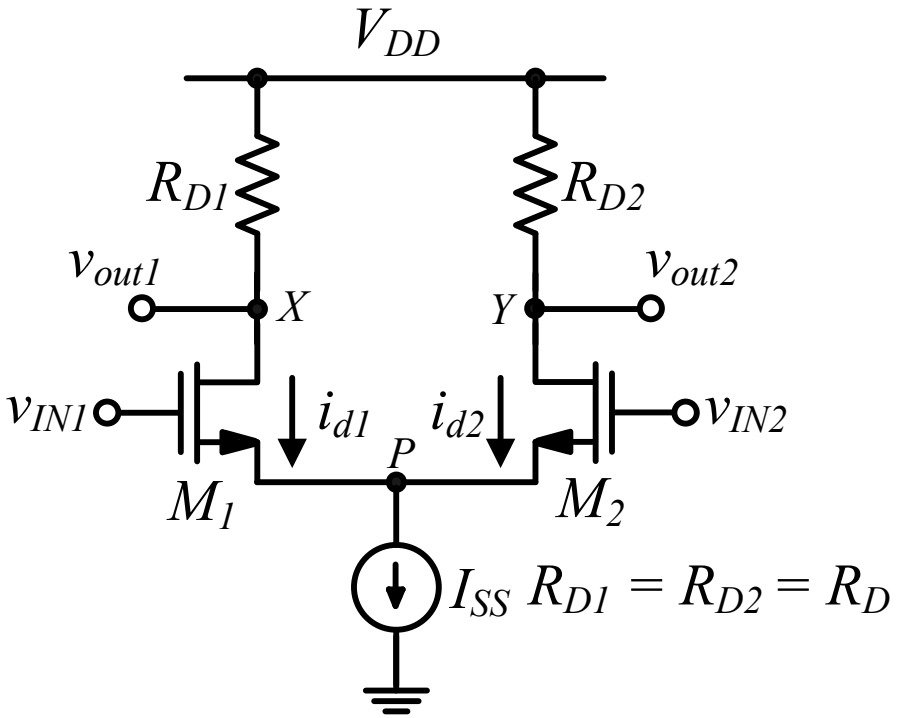


$$g_m = g_{m1} = g_{m2} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$$V_{outd} = V_{outd1} - V_{outd2} = -g_m R_D V_{id}$$

$$A_{vd} = \frac{V_{outd}}{V_{id}} = -g_m R_D$$

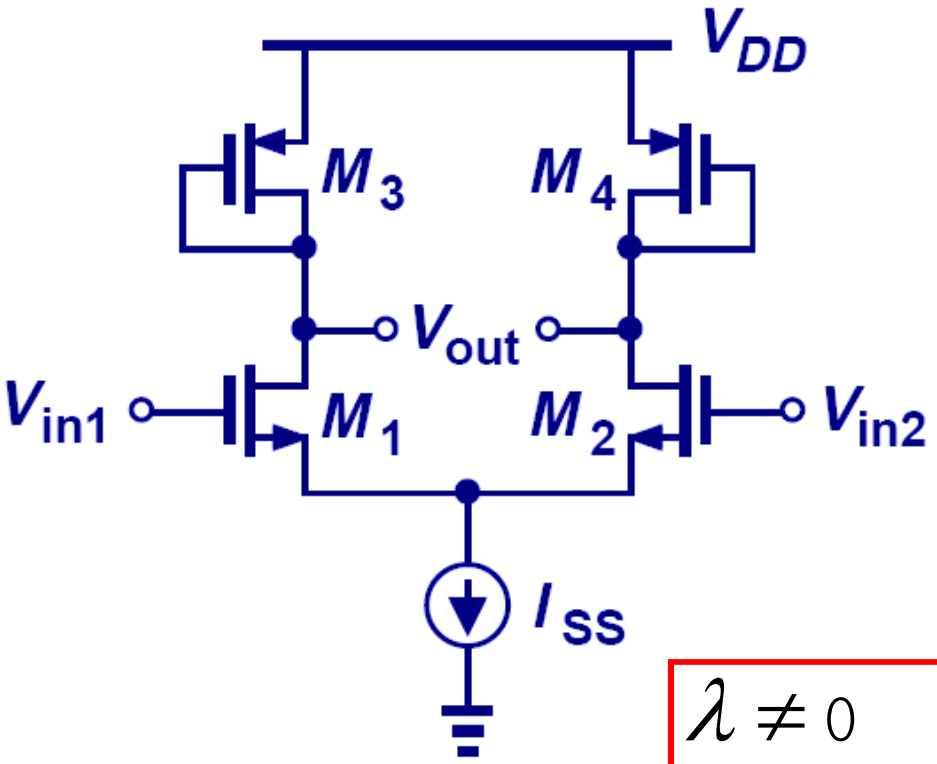
Small-Signal Response

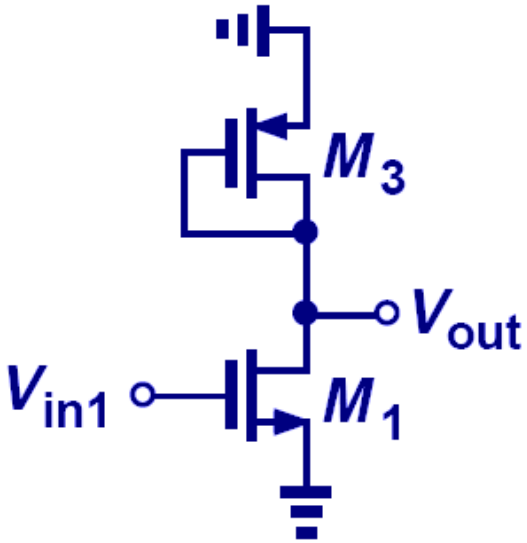


$$A_{vd} = -g_m R_D$$

- Similar to its bipolar counterpart, the MOS differential pair exhibits the same virtual ground node and small signal gain.

MOS Differential Pair Half Circuit Example I

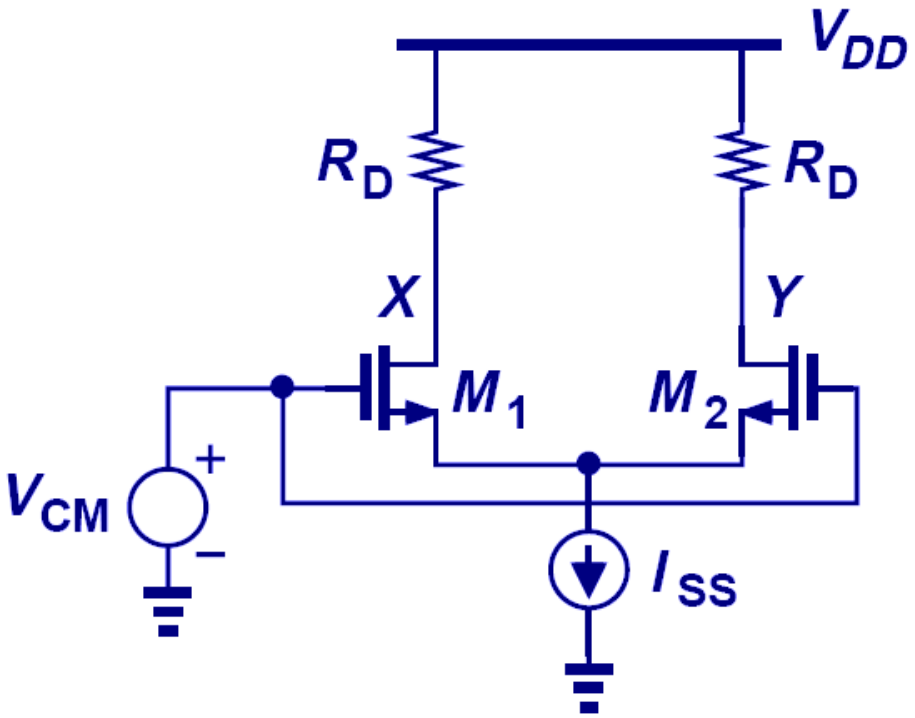




$$\lambda \neq 0$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O3} \| r_{O1}\right)$$

MOS Differential Pair's Common-Mode Response



$$V_{outc1} = V_{outc2} = V_{outc}$$

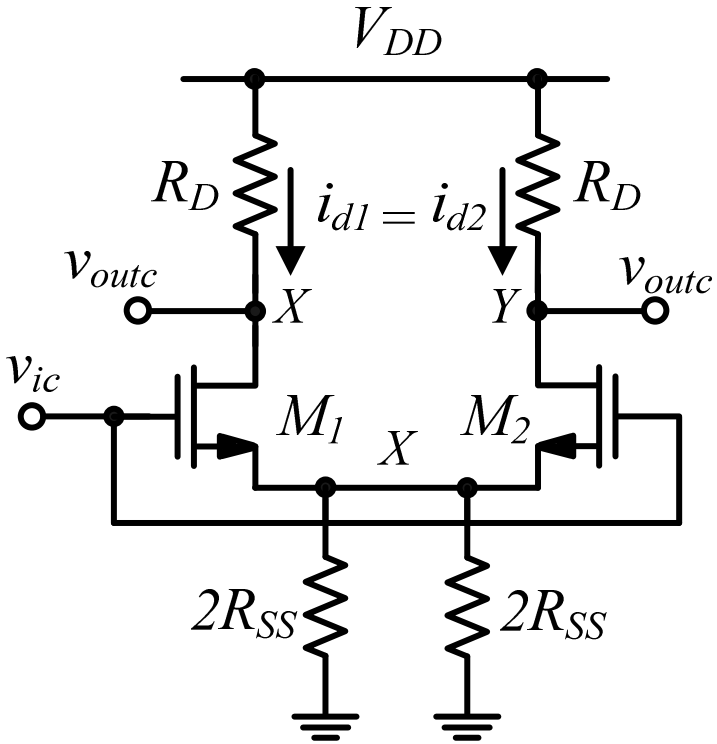
$$V_{outc1} = V_X, V_{outc2} = V_Y$$

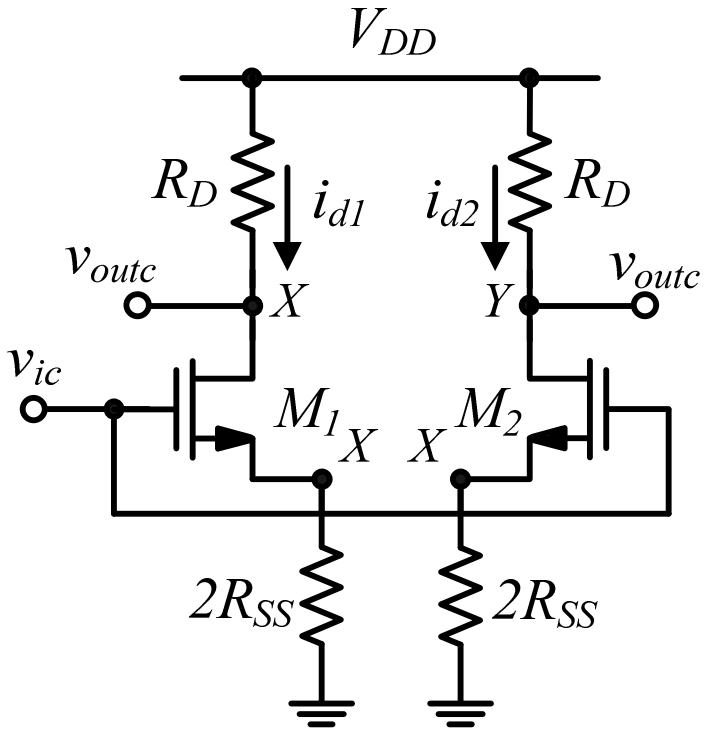
$$V_X = V_Y = V_{DD} - R_D \frac{I_{SS}}{2}$$

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

- Similar to its bipolar counterpart, MOS differential pair produces zero differential output as V_{CM} changes.

Common-Mode Response, $A_{CM\text{-}DM}$





CS Stage with Degeneration

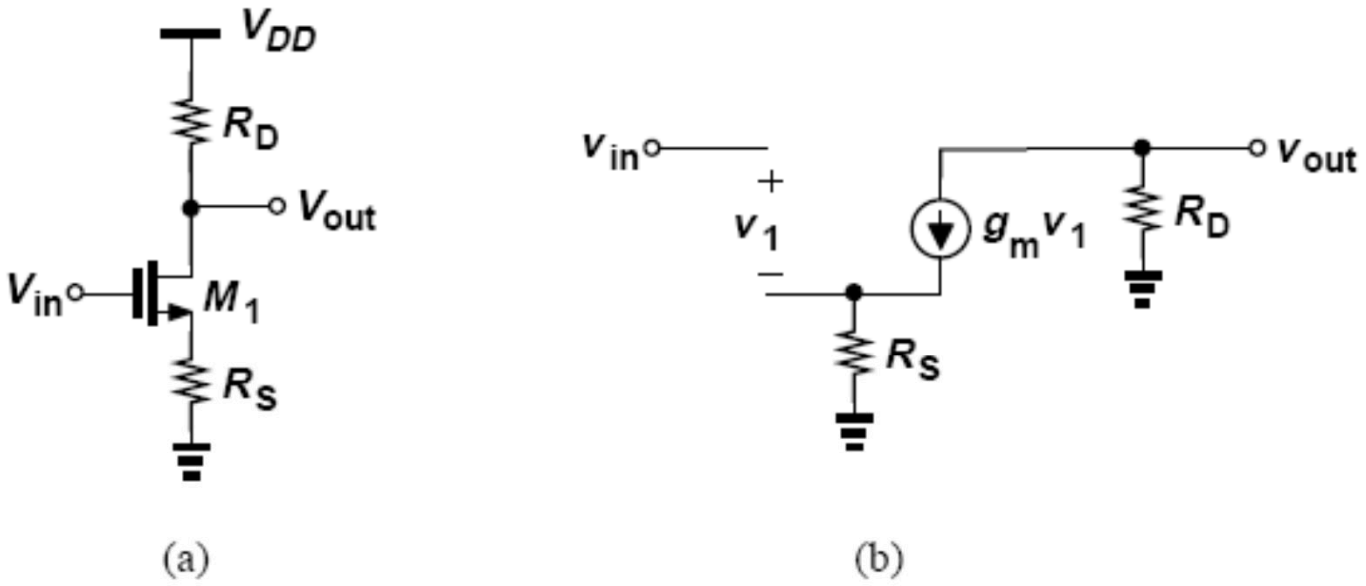


Figure 7.14 (a) CS stage with degeneration, (b) small-signal model.

$$v_{in} = v_1 + g_m v_1 R_S \tag{7.64}$$

and hence

$$v_1 = \frac{v_{in}}{1 + g_m R_S}. \tag{7.65}$$

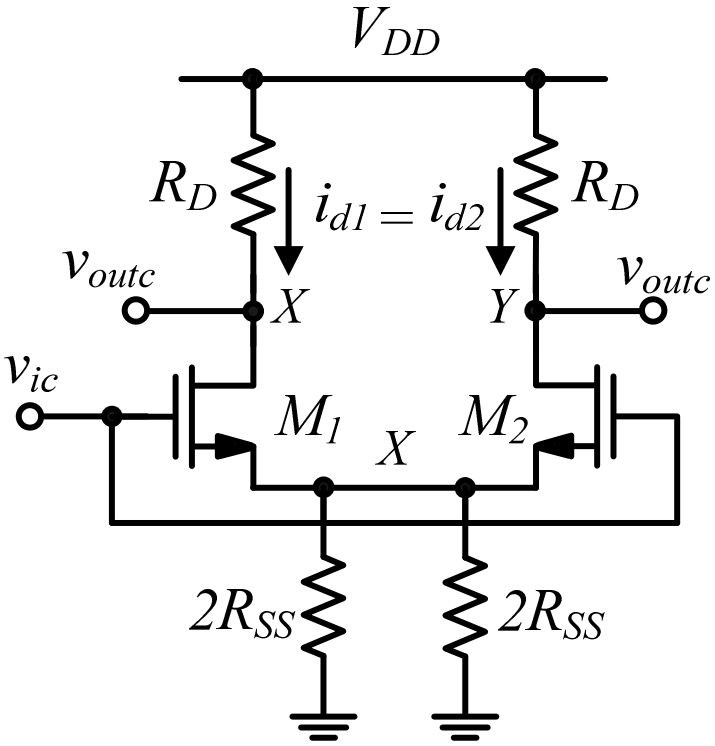
Since $g_m v_1$ flows through R_D, $v_{out} = -g_m v_1 R_D$ and

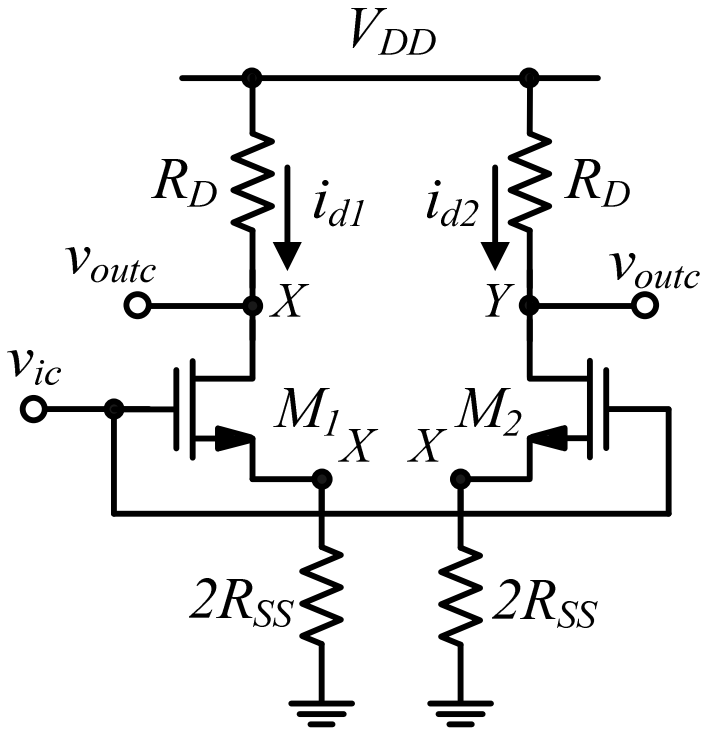
$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} \tag{7.66}$$

$$= -\frac{R_D}{\frac{1}{g_m} + R_S}, \tag{7.67}$$

a result identical to that expressed by (5.157) for the bipolar counterpart.

Common-Mode Response, $A_{CM\text{-}DM}$





$$V_{outc1} = V_{outc2} \cong -\frac{g_m R_D}{1 + 2g_m R_{SS}} V_{ic}$$

Common-Mode Response

$$A_{VC} = \frac{V_{outc}}{V_{ic}} \cong -\frac{g_m R_D}{1 + 2 g_m R_{SS}}$$

BJT Differential Amplifier.

- Differential Amplifier analysis
  - differential mode signal analysis
  - common mode signal analysis

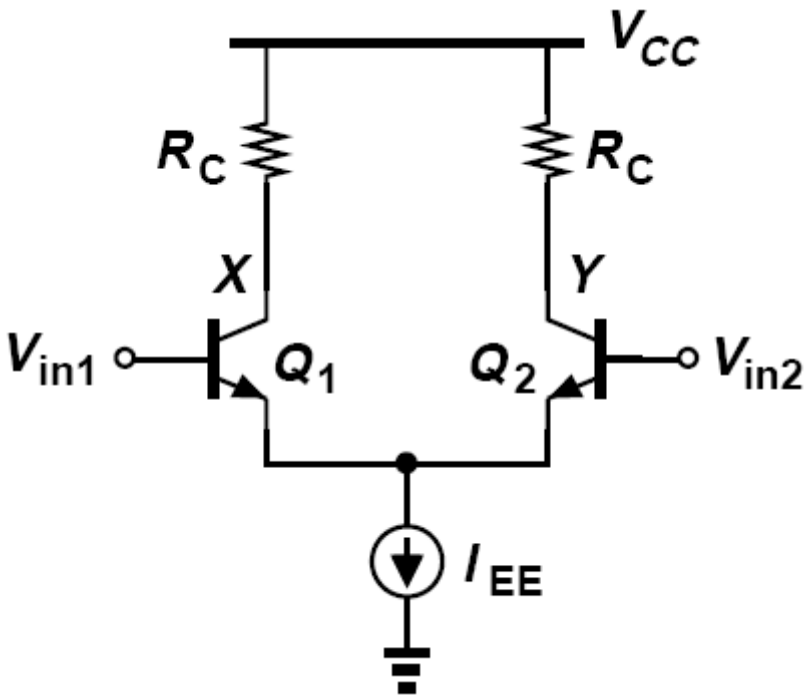
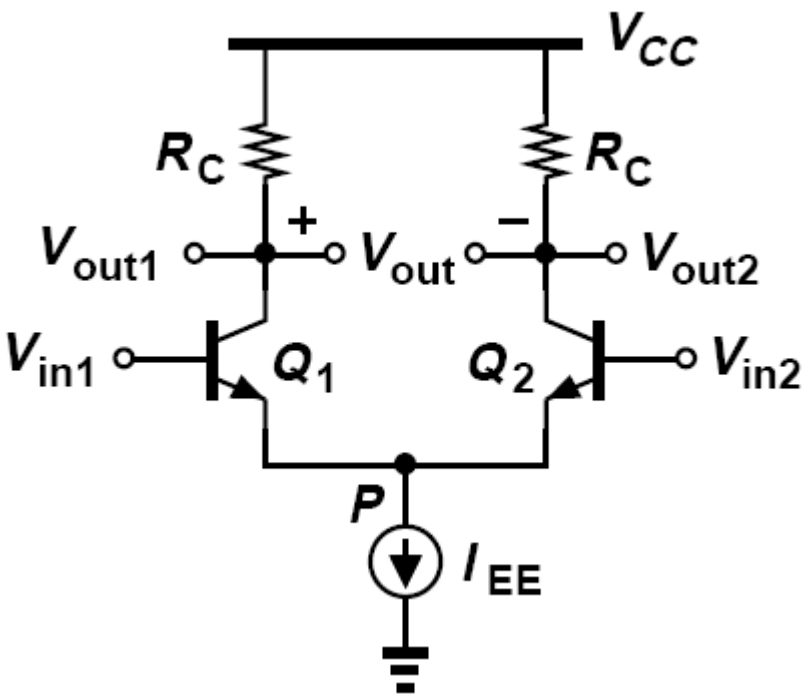


Fig. 7.12 The basic BJT differential-pair configuration.

Large Signal Analysis



$$V_{BE} = V_T \ln(I_C/I_S)$$

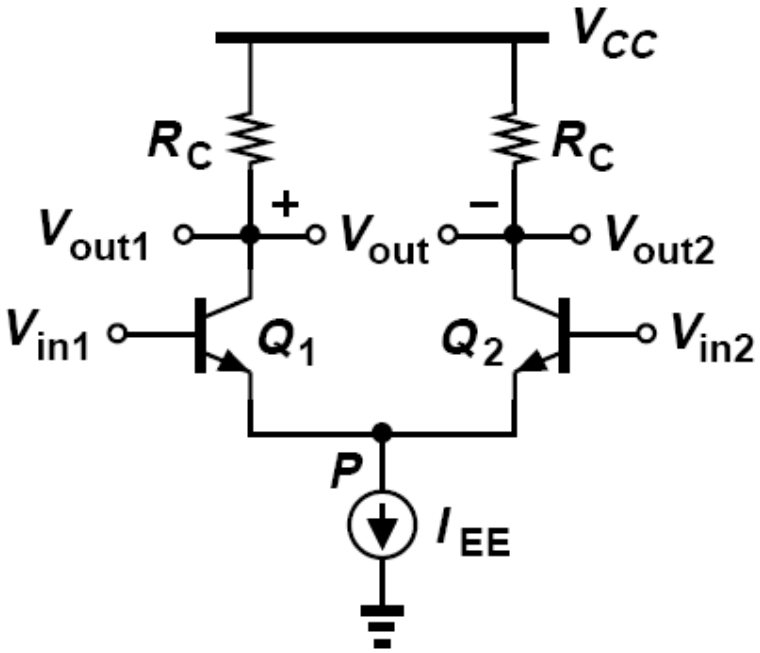
$$I_{C1} + I_{C2} = I_{EE}.$$

$$V_{out1} = V_{CC} - R_C I_{C1}$$

$$V_{out2} = V_{CC} - R_C I_{C2}$$

$$V_{out} = V_{out1} - V_{out2}$$

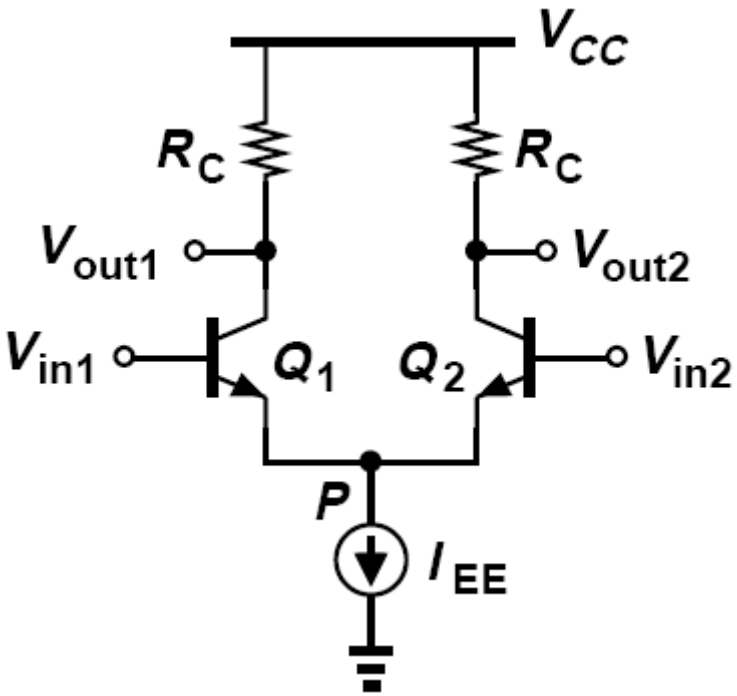
$$= -R_C(I_{C1} - I_{C2}).$$

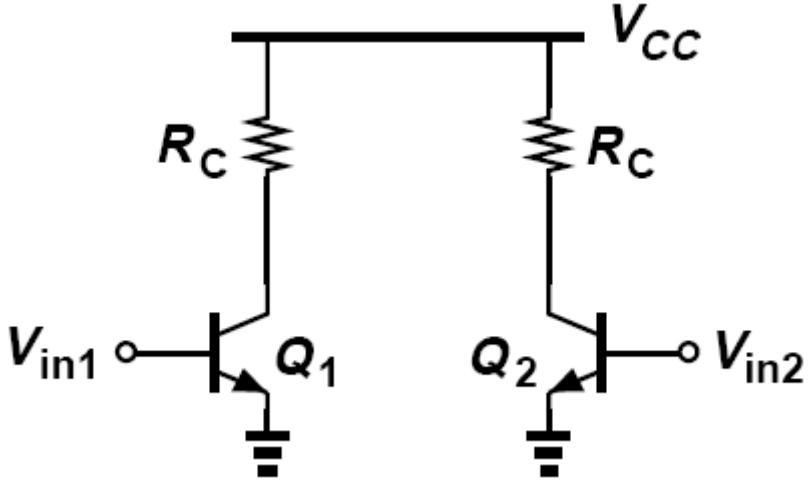


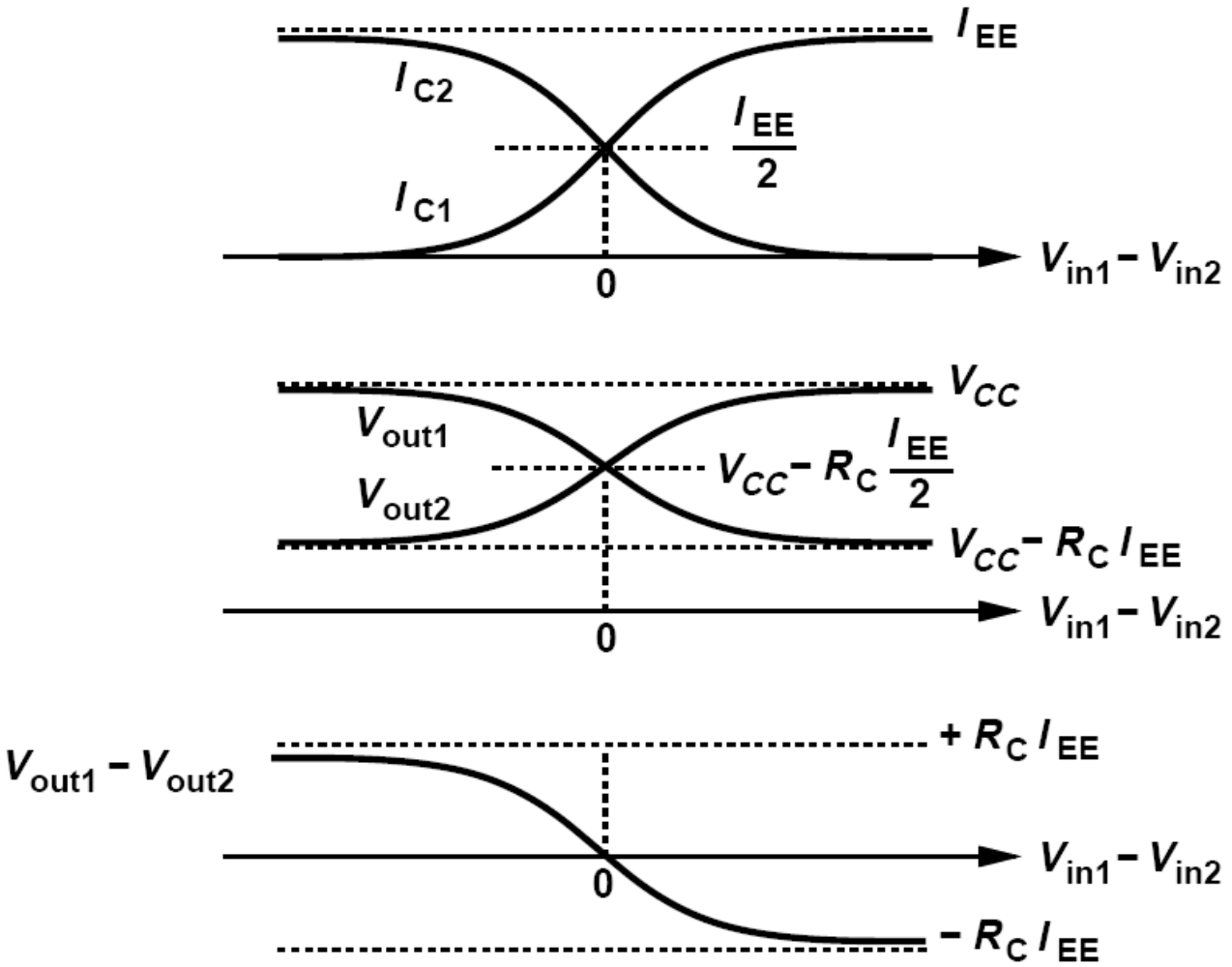
$$V_{in1} - V_{BE1} = V_P = V_{in2} - V_{BE2},$$

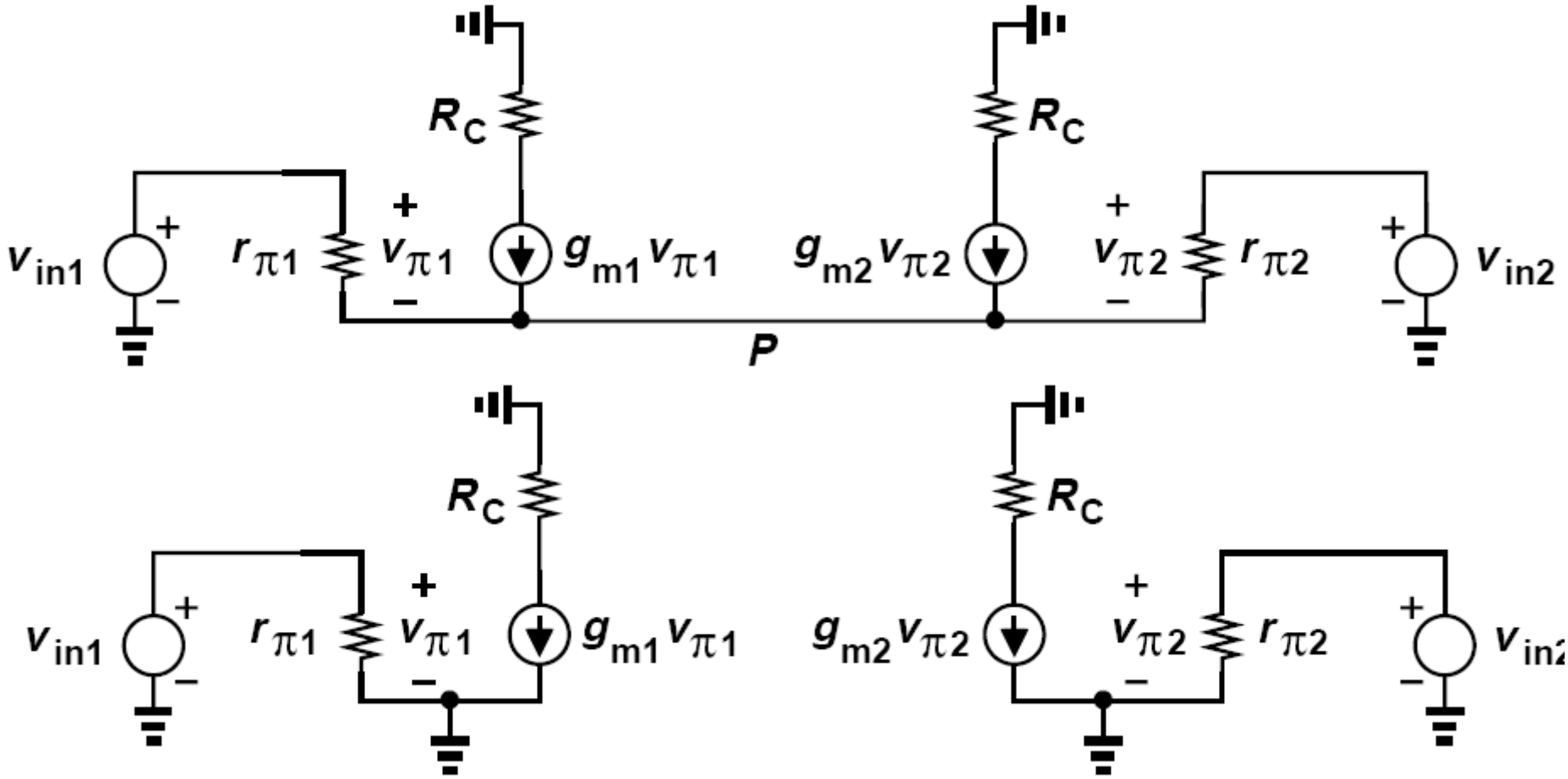
$$\begin{aligned} V_{in1} - V_{in2} &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}} \\ &= V_T \ln \frac{I_{C1}}{I_{C2}}. \end{aligned}$$

Small Signal Analysis






I_{EE}
I_{C2}
$\frac{I_{EE}}{2}$
I_{C1}
0
$V_{in1} - V_{in2}$
V_{CC}
V_{out1}
$V_{CC} - R_C \frac{I_{EE}}{2}$
V_{out2}
$V_{CC} - R_C I_{EE}$
0
$V_{in1} - V_{in2}$
$V_{out1} - V_{out2}$
$+ R_C I_{EE}$
$V_{in1} - V_{in2}$
0
$- R_C I_{EE}$


R_C
R_C
v_{in1}
$r_{\pi 1}$
$v_{\pi 1}$
$g_{m1} v_{\pi 1}$
$g_{m2} v_{\pi 2}$
$v_{\pi 2}$
$r_{\pi 2}$
v_{in2}
P
R_C
R_C
v_{in1}
$r_{\pi 1}$
$v_{\pi 1}$
$g_{m1} v_{\pi 1}$
$g_{m2} v_{\pi 2}$
$v_{\pi 2}$
$r_{\pi 2}$
v_{in2}

$$v_{in1} - v_{\pi 1} = v_P = v_{in2} - v_{\pi 2}$$

$$\frac{v_{\pi 1}}{r_{\pi 1}} + g_{m1} v_{\pi 1} + \frac{v_{\pi 2}}{r_{\pi 2}} + g_{m2} v_{\pi 2} = 0.$$

With $r_{\pi 1} = r_{\pi 2}$ and $g_{m1} = g_{m2}$, (10.82) yields

$$v_{\pi 1} = -v_{\pi 2}$$

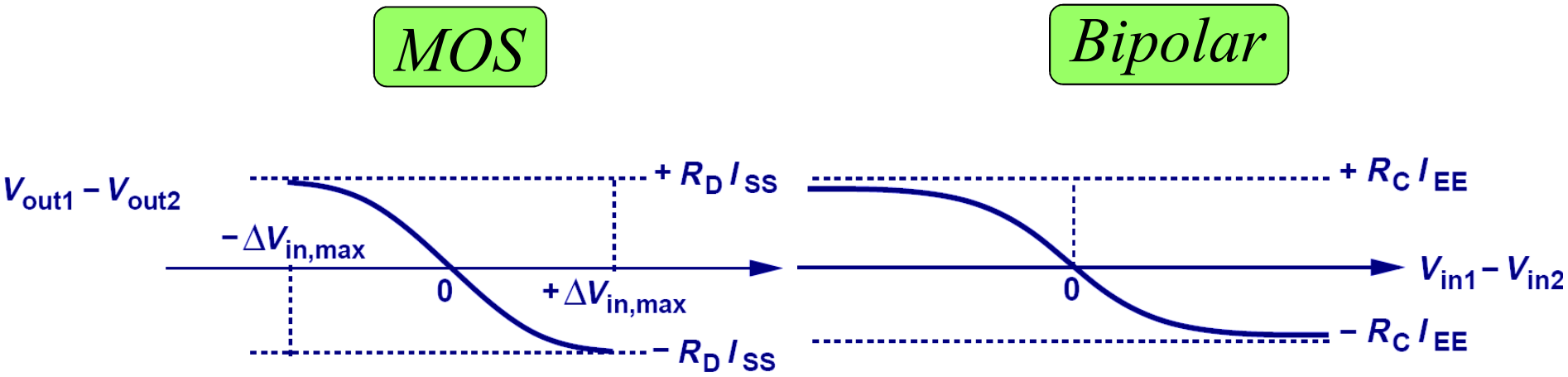
and since $v_{in1} = -v_{in2}$, (10.81) translates to

$$v_{out1} = -g_m R_C v_{in1}$$

$$v_{out2} = -g_m R_C v_{in2}.$$

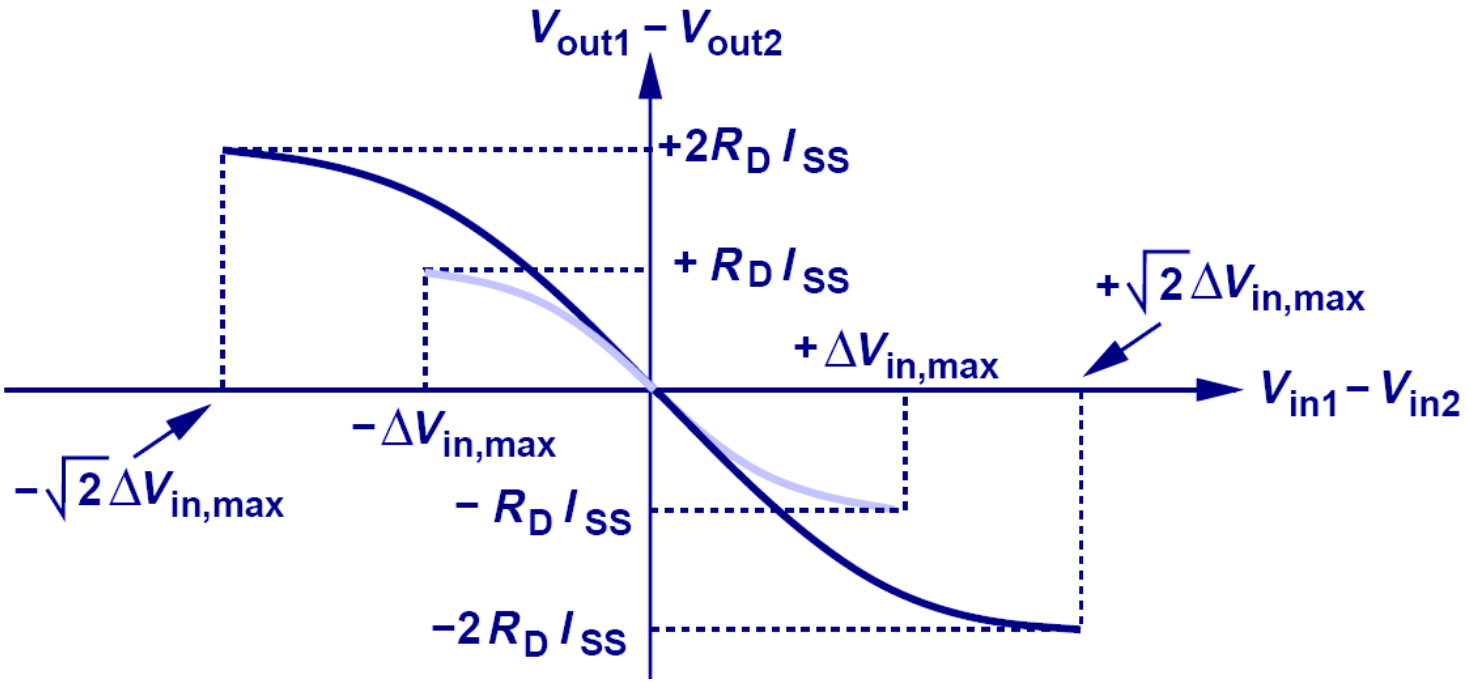
$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m R_C$$

Contrast Between MOS and Bipolar Differential Pairs



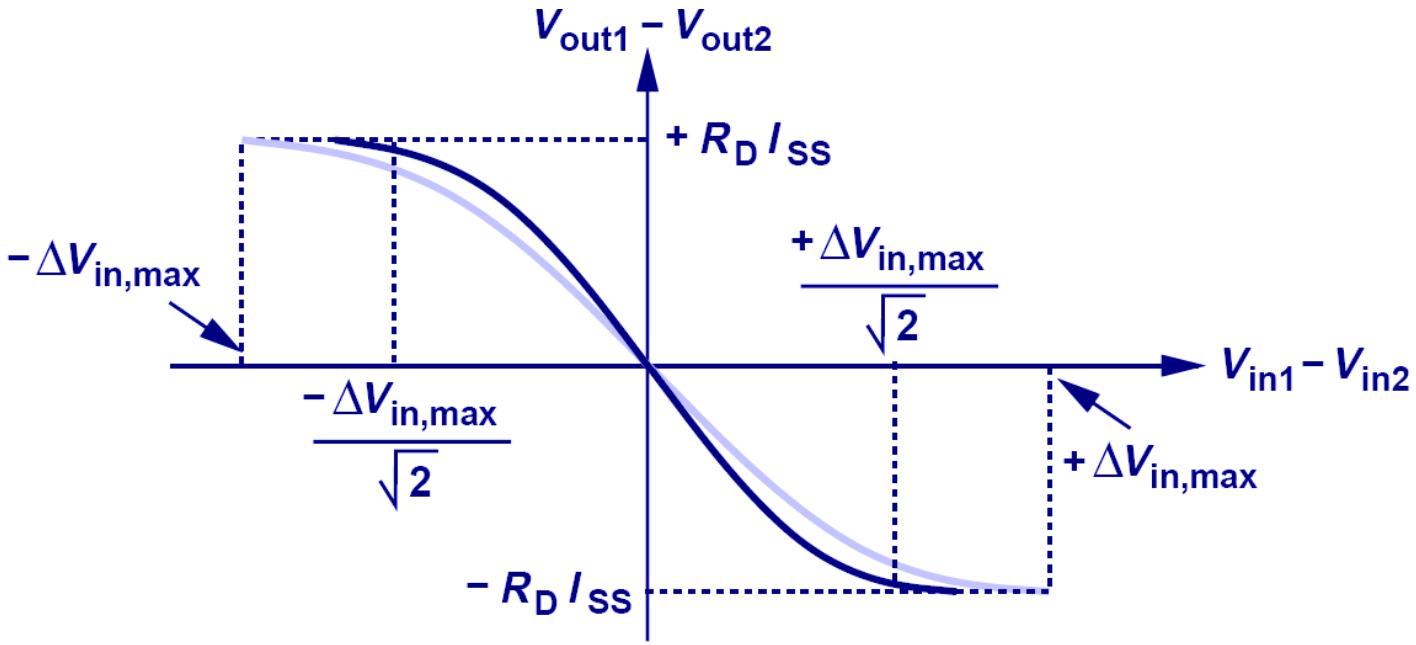
- In a MOS differential pair, there exists a finite differential input voltage to completely switch the current from one transistor to the other, whereas, in a bipolar pair that voltage is infinite.

The effects of Doubling the Tail Current



- Since I_{SS} is doubled and W/L is unchanged, the equilibrium overdrive voltage for each transistor must increase by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ increases by $\sqrt{2}$ as well. Moreover, since I_{SS} is doubled, the differential output swing will double.

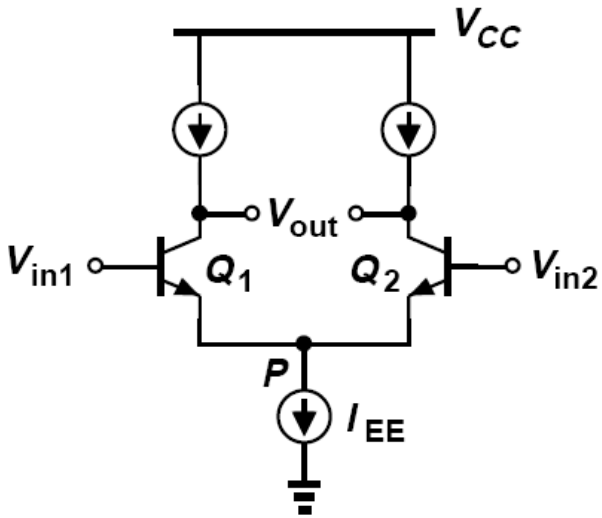
The effects of Doubling W/L

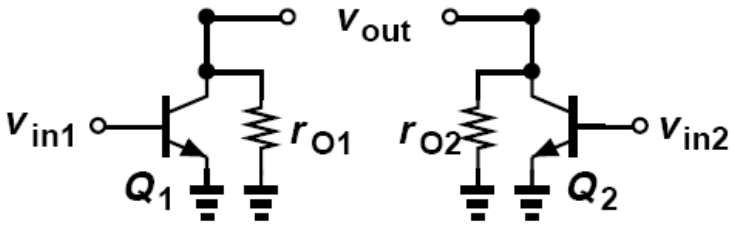


- Since W/L is doubled and the tail current remains unchanged, the equilibrium overdrive voltage will be lowered by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ will be lowered by $\sqrt{2}$ as well. Moreover, the differential output swing will remain unchanged since neither I_{SS} nor R_D has changed

Example 10.10

Compute the differential gain of the circuit shown in Fig. 10.16(a), where ideal current sources are used as loads to maximize the gain.





Solution

With ideal current sources, the Early effect in Q_1 and Q_2 cannot be neglected, and the half circuits must be visualized as depicted in Fig. 10.16(b). Thus,

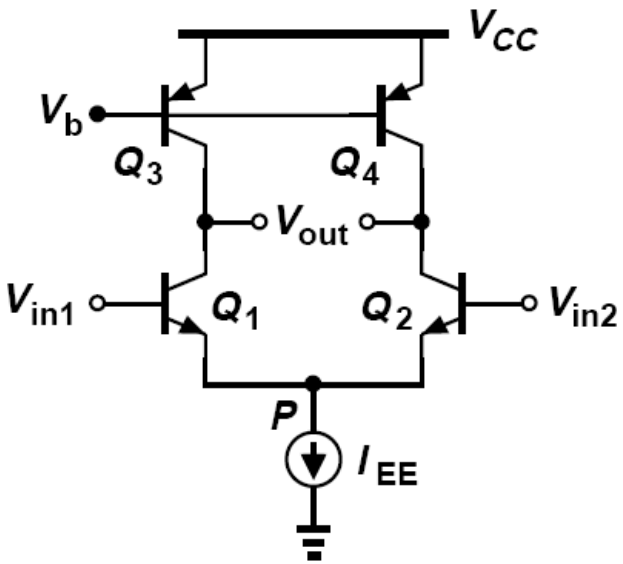
$$v_{out1} = -g_m r_O v_{in1} \tag{10.90}$$

$$v_{out2} = -g_m r_O v_{in2} \tag{10.91}$$

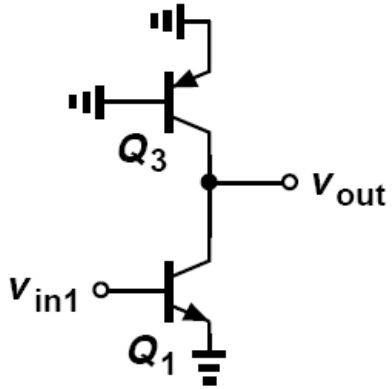
$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m r_O .$$

Example 10.11

Figure 10.17(a) illustrates an implementation of the topology shown in Fig. 10.16(a). Calculate the differential voltage gain.



(a)



(b)

Solution

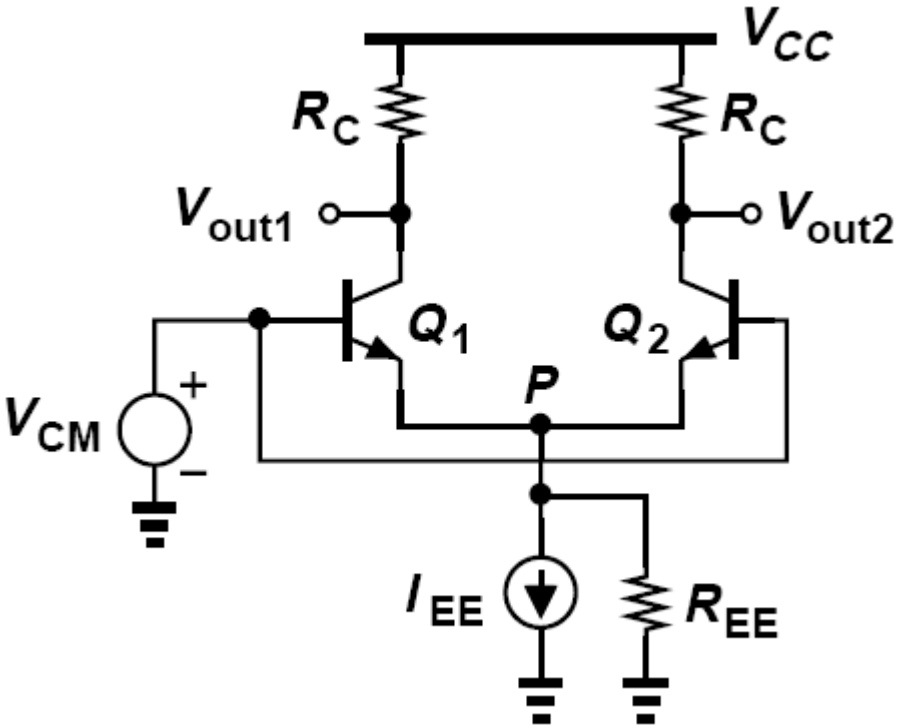
Noting that each pnp device introduces a resistance of r_{OP} at the output nodes and drawing the half circuit as in Fig. 10.17(b), we have

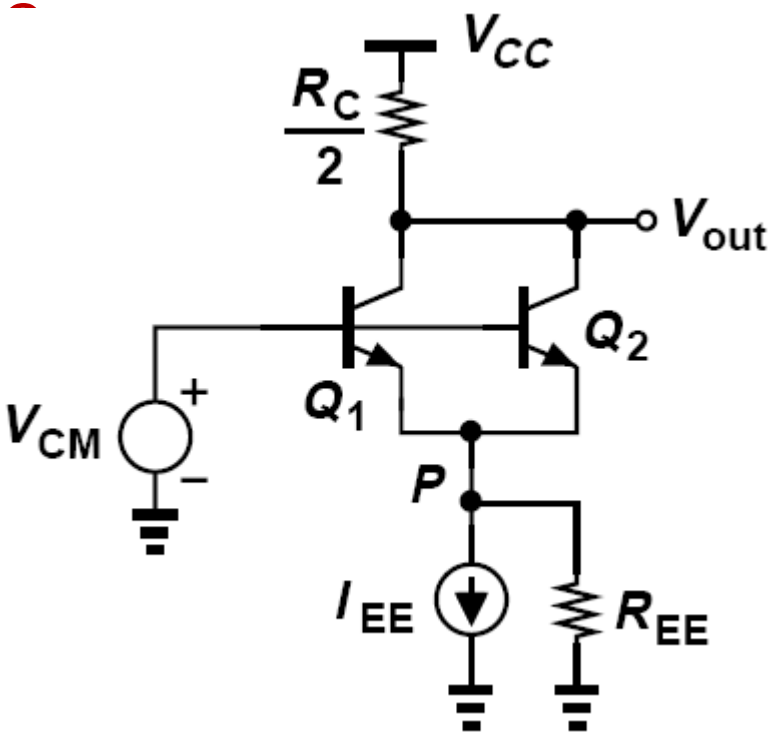
$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m(r_{ON}||r_{OP}),$$

where r_{ON} denotes the output impedance of the npn transistors.

Exercise

Calculate the gain if Q_3 and Q_4 are configured as diode-connected devices.





$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{\frac{R_C}{2}}{R_{EE}+\frac{1}{2g_m}}$$

$$= -\frac{R_C}{2R_{EE}+g_m^{-1}},$$

$$A_{VC} = \frac{V_{outc}}{V_{CM}} \cong -\frac{g_m R_C}{1+2g_m R_{EE}}$$

Common Mode Rejection Ratio : CMRR

- **Common mode rejection ratio (CMRR)** คือ อัตราการกำจัดสัญญาณโหมดร่วม

$$CMRR = \left| \frac{A_{vd}}{A_{vc}} \right|$$

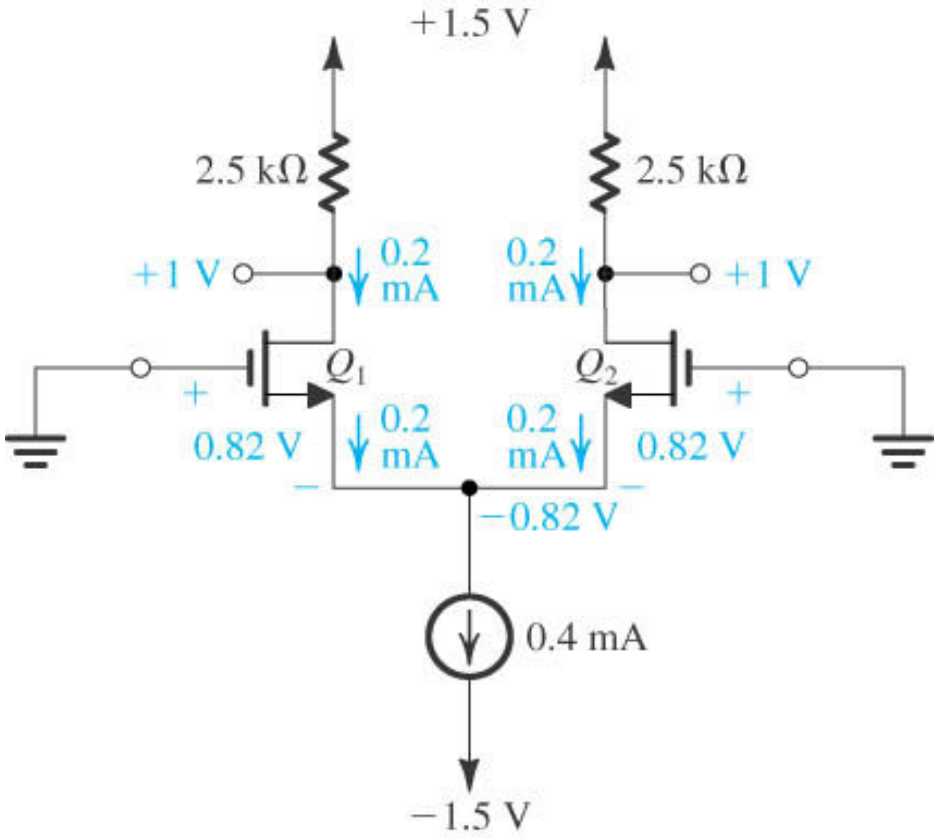
MOSFET

$$CMRR = 1 + 2g_m R_{SS}$$

BJT

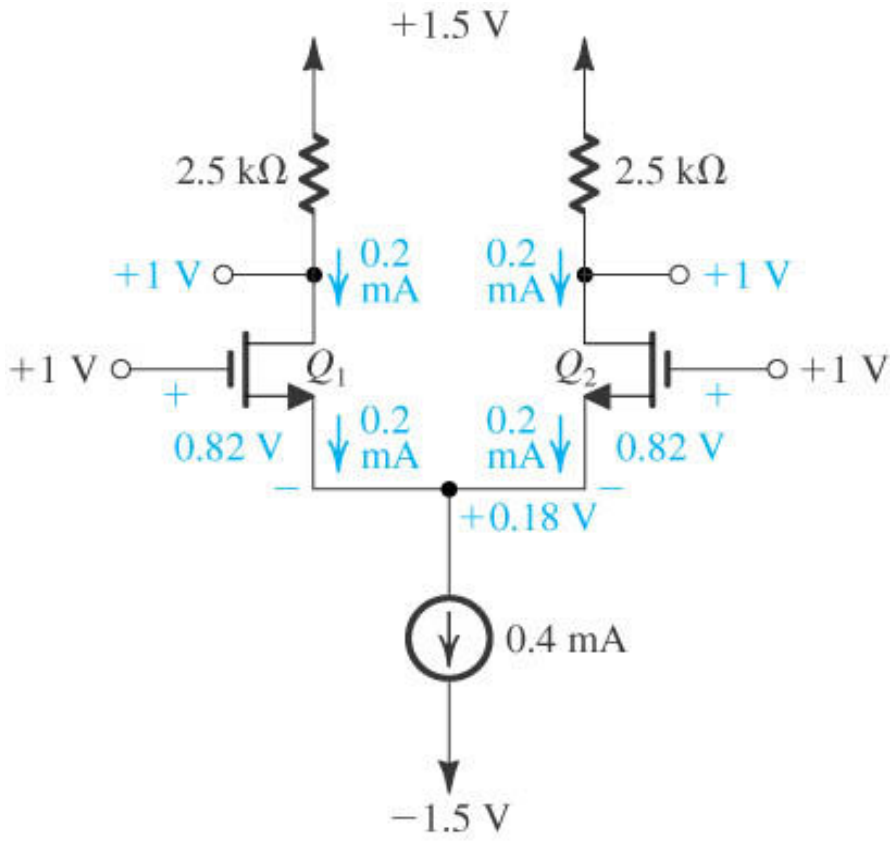
$$CMRR = 1 + 2g_m R_{EE}$$

Ex 7.1 V_{DD}=V_{SS}=1.5 V, R_D = 2.5 k and M_1= M_2 has K_N = 2 mA/V^2
V_{TH} = 0.5 V and I_{SS} = 0.4 mA Find V_{out}

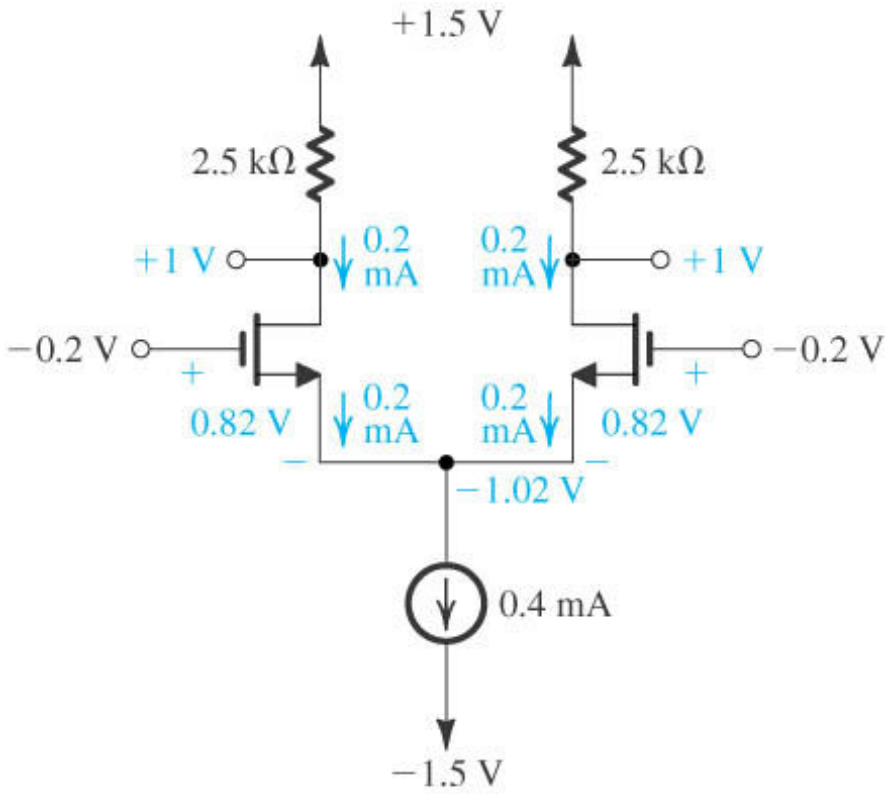


(a)

Ex 7.2 V_{DD}=V_{SS}=1.5 V, R_D = 2.5 k and M_1= M_2 has K_N = 2 mA/V^2
V_{TH} = 0.5 V and I_{SS} = 0.4 mA Find V_{out}



Ex 7.3 V_{DD}=V_{SS}=1.5 V, R_D = 2.5 k and M_1= M_2 has K_N = 2 mA/V^2
V_{TH} = 0.5 V and I_{SS} = 0.4 mA Find V_{out}



(c)

Offset Voltage to compensate

- สาเหตุที่เกิดแรงดันออฟเซตคือค่าความต้านทานของโหลด และค่า K_N และ V_{TH} ของมอสที่เป็นคู่ผลต่างไม่เท่ากัน

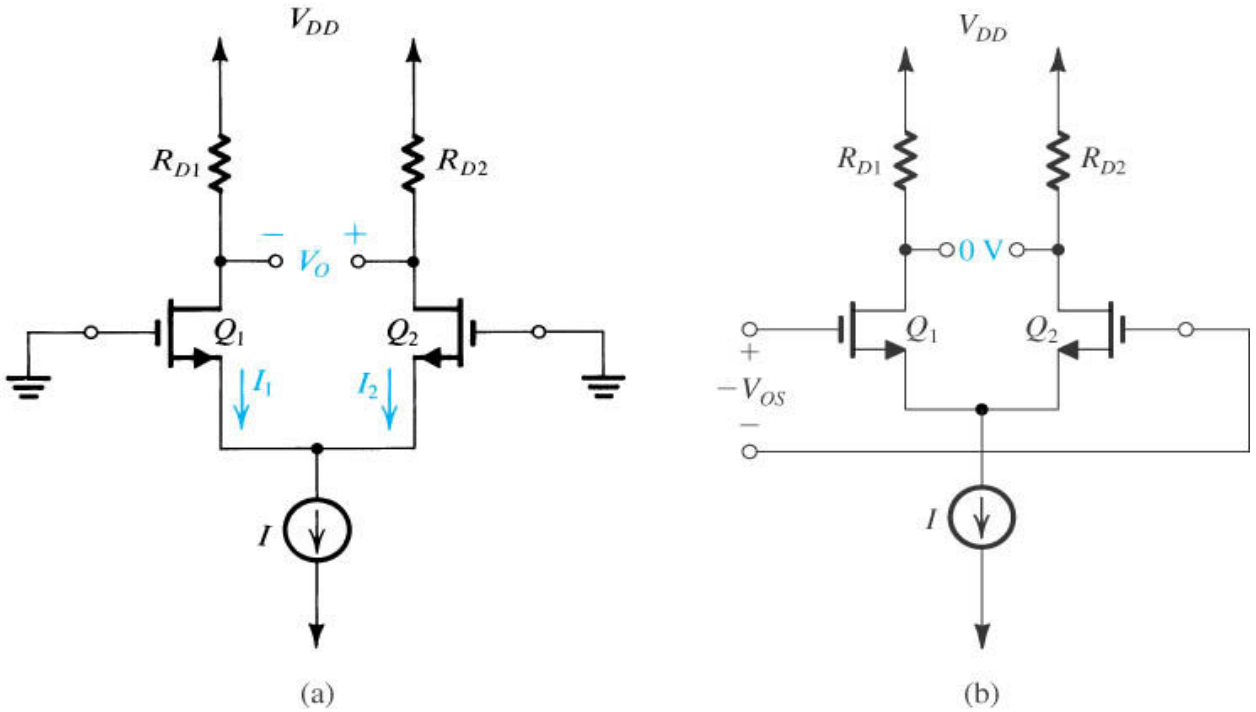
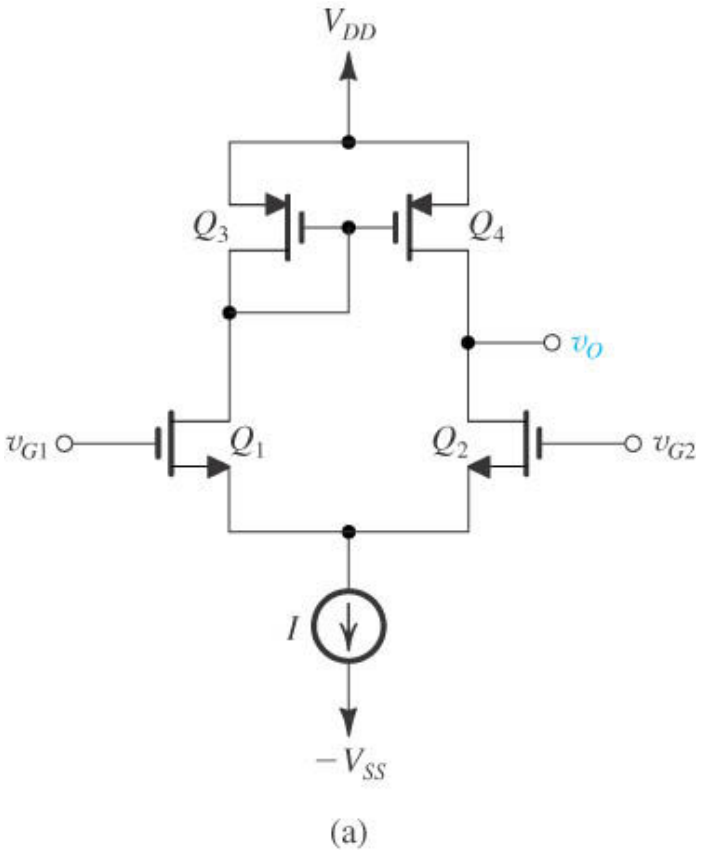


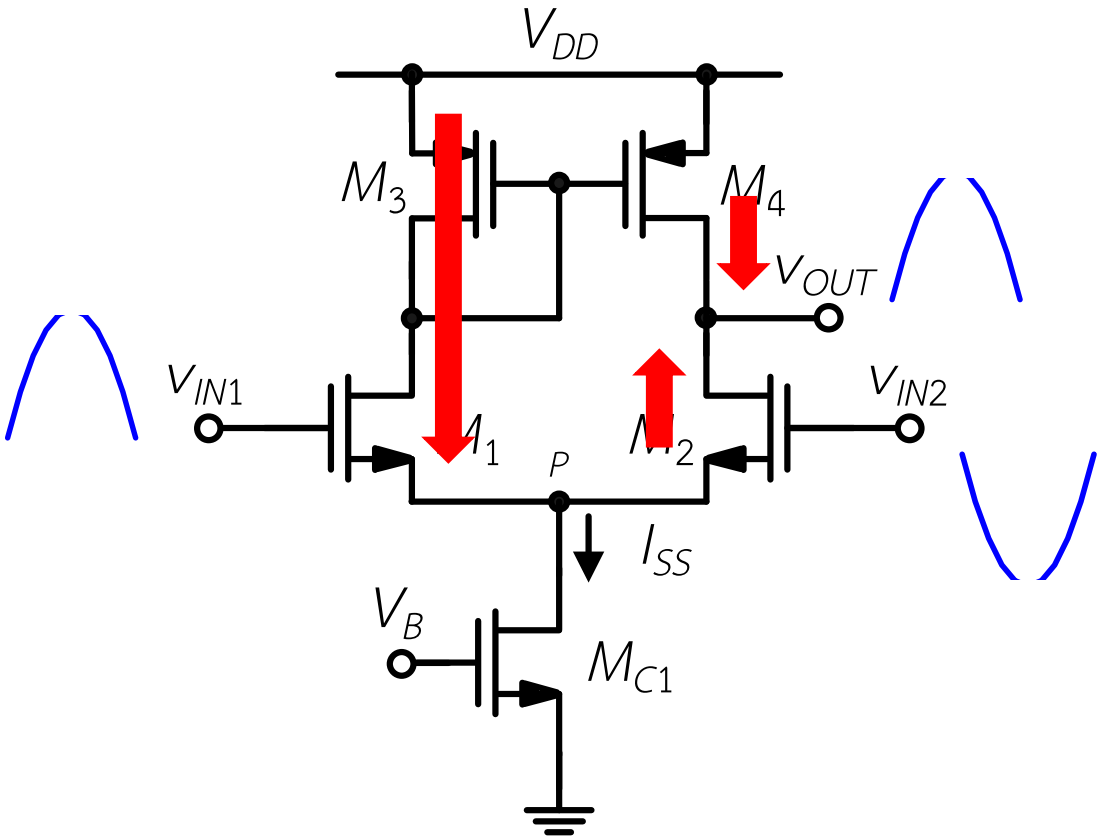
Figure 7.25 (a) The MOS differential pair with both inputs grounded. Owing to device and resistor mismatches, a finite dc output voltage V_O results. (b) Application of a voltage equal to the input offset voltage V_{OS} to the terminals with opposite polarity reduces V_O to zero.

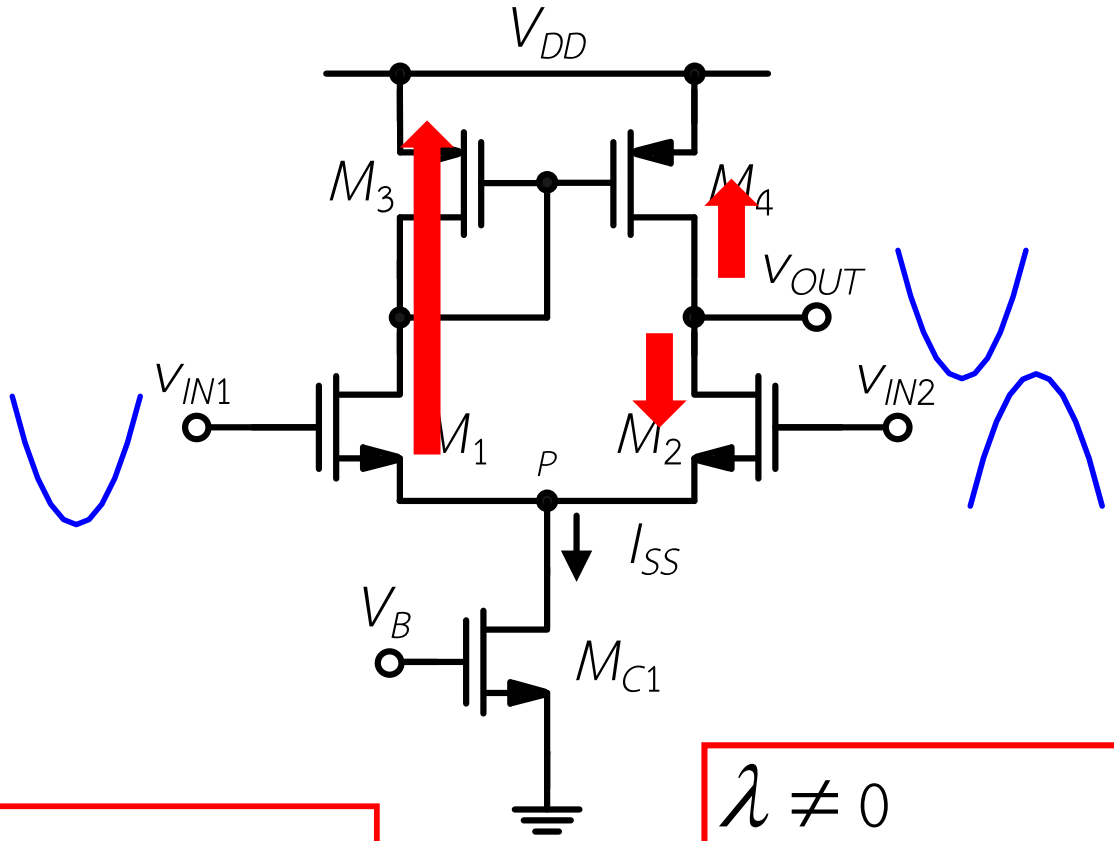
Active Loads

- Active load maintains bias current I
- Active load has high impedance



(a)


V_{DD}
M_3
M_4
V_{OUT}
V_{IN1}
V_{IN2}
M_1
M_2
P
I_{SS}
V_B
M_{C1}



$$\lambda \neq 0$$

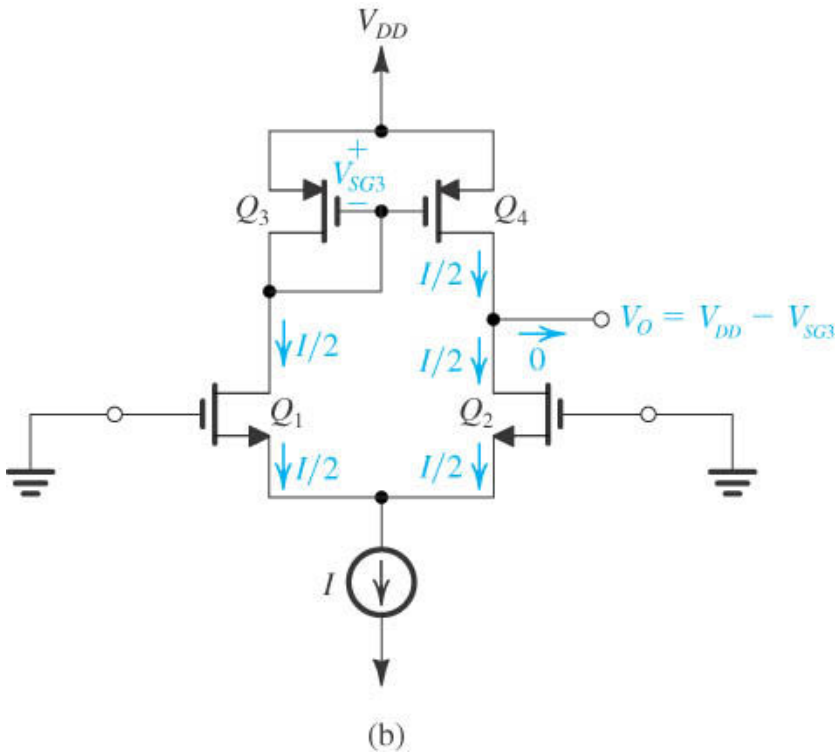
$$A_{vd} = -g_{m1,2}\left(r_{O3} \parallel r_{O2}\right)$$

$$\lambda \neq 0$$

$$A_{vc} = \frac{-g_{m1,2}\left(r_{O3} \parallel r_{O2}\right)}{1 + g_{m1,2}\left(r_{O3} \parallel 2r_{O2}R_{SS}\right)}$$

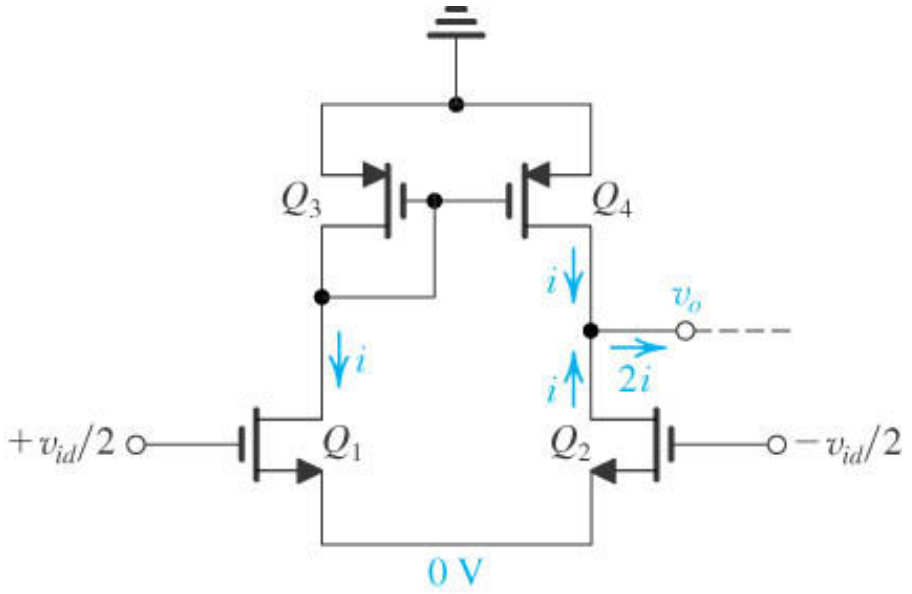
Active Load

- Active Load in Saturation
- Without any input



Active Load

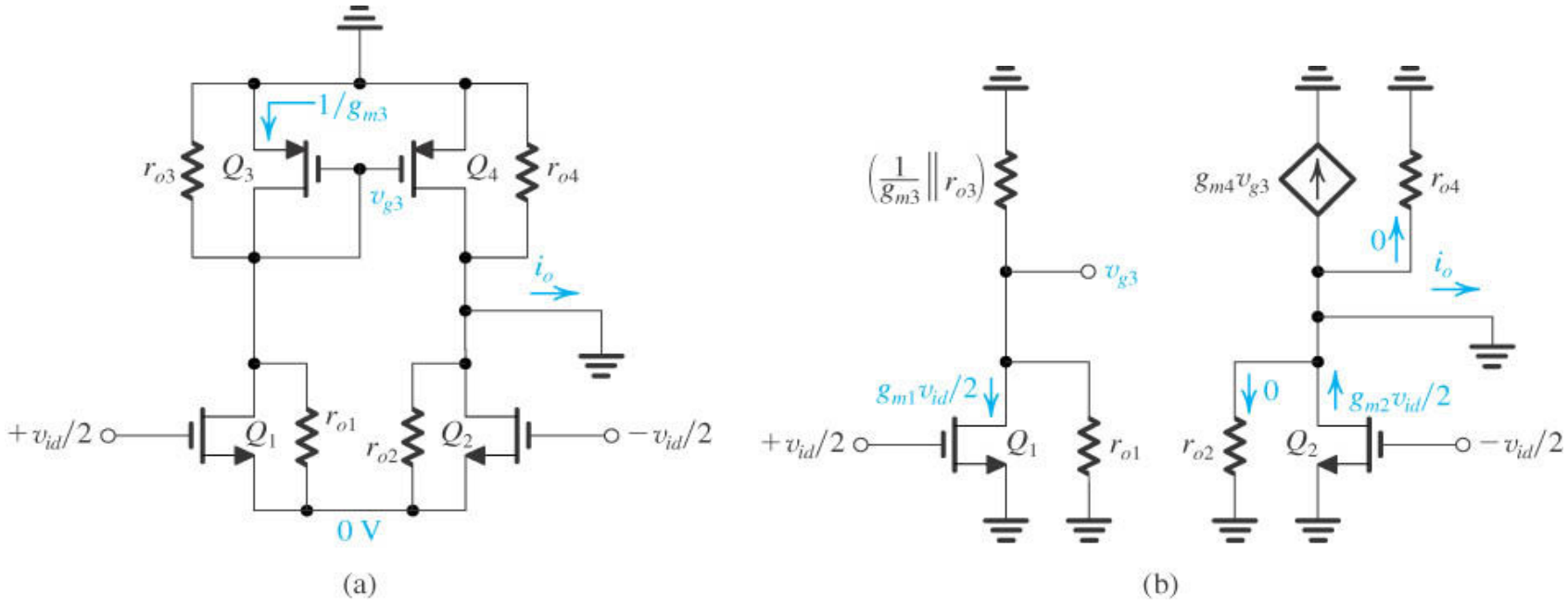
- The current generated by differential input will only flow to the load



(c)

Active Load

- In practice, leakage from Drain to Source



Reference

1. Adel S. Sedra, Kenneth C. Smith "Microelectronic Circuit"
2. Pual R. Gray and Robert G. Mayer "Analysis and Design of Integrated Circuit"

Thank you