Feedforward Bulk-Driven Class AB Fully-Differential Second-Generation Current Conveyor (FDCCII)

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Abstract. In this paper, a feedforward bulk-driven class AB fully-differential second-generation current conveyer (FDCCII) is presented. Bulk-driven differential pair is employed for the input stage allowing the FDCCII to operate with rail-to-rail operation. Feedfoward technique is also incorporated into input stage to increase the DC gain and minimize the common mode gain. The circuit performance is verified using HSPICE in 0.18 μm CMOS technology. The simulation results show rail-to-rail input and output swings. The DC voltage transfer characteristic between ports Y and X and DC current transfer characteristic between ports X and Z shows good linearity. The bandwidths show 25.7 MHz (V_X/V_Y), 30 MHz (I_Z/I_X), respectively. The power dissipation is 267.5 μW.

INTRODUCTION

The second generation current conveyor (CCII) is one of the versatile current-mode building blocks [1]. CCII has been used in a wide range of applications such as current amplifier, filter, oscillator, instrumentation, and variable gain amplifier. Nowadays, various portable equipments have become increasingly important. Therefore the circuit operating at low voltage with rail-to-rail (RR) operation is necessary [2-3]. It is also well known that fully balanced differential operation can improve the dynamic range, harmonic distortion and noise performance of the circuit.

Several CCIIs have been proposed [4-9]. The CCII using differential amplifier technique [4] operates from a 6.6 volt with limited input and output swings. To achieve a low voltage and RR operation, bulk-driven and folded cascode techniques have been reported and the resulting CCII demonstrates low supply voltage operation [5]. However, since the bulk transconductance is 2 to 5 times lower than the gate transconductance, the dc gain is still low and as a result the impedance at port X is high. The floating gate MOS (FG-MOS) transistor CCII has been proposed and can operate from a 1.6 supply voltage [6]. The impedance at port X is still quite high causing the voltage transfer problem between ports Y and X. Fully differential CCII (FDCCII) has been proposed [7-8]. Unfortunately, their architectures do not support RR operation making them unsuitable for low-voltage mixed-mode integrated circuits whose noise is a major concern.

This paper presents a FDCCII. The bulk-driven and feedforward techniques are used to enhance the transconductance and differential gain while suppress the common-mode gain. The paper is organized as follows. The proposed FDCCII is first presented. The circuit operation is then explained. Finally, the simulation results, discussions and conclusion are provided.

FULLY DIFFERENTIAL SECOND GENERATION CURRENT CONVEYER

Fig. 1 shows the proposed FDCCII while Fig. 2(a) shows the circuit symbol. Basically, FDCCII has high impedance at ports Y and Z while the impedance at port X is low. The transfer characteristic of FDCCII can be described as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

where I_X, I_Y, I_Z, V_X, V_Y, and V_Z are differential current and voltage at ports X, Y and Z, respectively, and given as $I_X = I_{X+}-I_{X-}$, $I_Y = I_{Y+}-I_{Y-}$, $I_Z = I_{Z+}-I_Z$, $V_X = V_{X+}-V_{X-}$, $V_Y = V_{Y+}-V_{Y-}$ and $V_Z = V_{Z+}-V_{Z-}$.

PROPOSED BULK-DRIVEN CMOS FDCCII

Bulk-driven CMOS FDCCII

The FDCCII comprises bulk-driven input differential pair $M_{1a,b}$-$M_{2a,b}$. $R_{G1(2)}$ is used to set the first-stage gain and bias the second stage amplifier which consists of quasi floating gate (QFG) transistors $M_{4a,b}$ and $M_{5a,b}$. $C_{G1a(b)}$ is used to pass the signal from the gate of $M_{4a(b)}$ to the gate of $M_{5a(b)}$ making the second stage amplifier operating in class AB [9]. QFG $M_{6a,b}$ and $M_{7a,b}$, which also operate in class AB, transfer the current from port X to port Z. The feedforward transconductor G_{mF} serves the purpose of enhancing the differential gain by increasing the effective bulk transconductance and suppressing the common-mode gain by appropriately compensating the bulk and gate transconductances. G_{mF}, as shown in Fig. 2(b), comprises a simple bulk-driven differential pair. In this design, $R_{GF1(2)}$ is used to set the differential gain while the common mode gain is determined by properly sizing the transistors M_3 and M_4. $R_{C1a(b)}$ and $C_{C1a(b)}$ are used to compensate the amplifier to ensure sufficient phase margin.

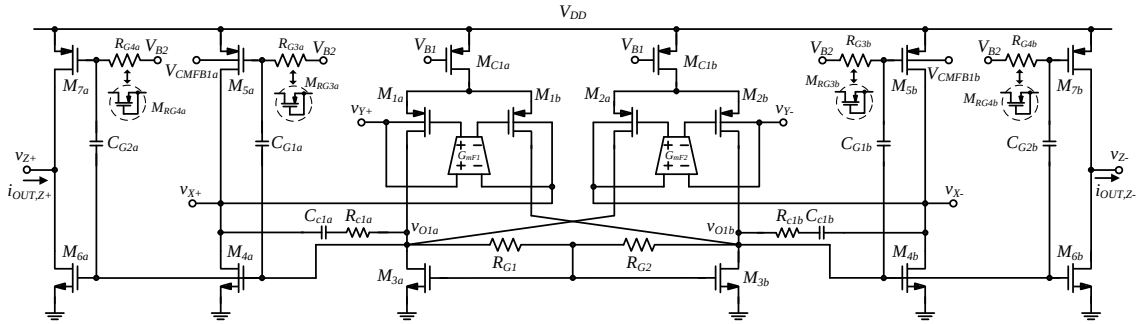


Fig. 1. Bulk-driven CMOS FDCCII with feedforward circuit.

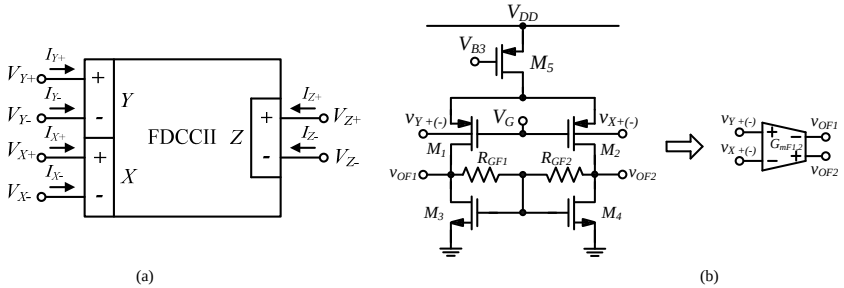


Fig. 2. (a) The Symbol of FDCCII and (b) bulk-driven feedforward transconductor.

The operation of the circuit can be explained as follows. When the input signal is differential, the current from two differential pairs are constructively combined. Note that the differential input signal is also passed through the feedforward amplifier G_{mF} which is arranged such that the output voltages of G_{mF1} and G_{mF2} are in phase with the input voltages and thus enhancing the effective transconductance of the differential pair G_{md}, i.e., $G_{md} \approx g_{mb1a(b)}+g_{m1a(b)}G_{mF}R_{GF1(2)}$ where g_{mb} and g_m are the bulk and gate transconductance, respectively. The first-stage differential gain is therefore given by $G_{md}R_{G1(2)}$. In case of the common mode signal, G_{mF} will produce the signals at the gates of $M_{1a(b)}$ and $M_{2a(b)}$ which are in opposite phase with the input signals. As a result, the currents produced by $M_{1a(b)}$ and $M_{2a(b)}$ are much reduced. Straight forward small signal analysis shows that the common mode gain is $A_{vc} \approx [(1/2r_{oc1})-(1/4g_{m3}r_{oc1}r_{o5})]/g_{m3a(b)}$. Obviously, $R_{G1(2)}$ plays role in determining the differential gain while the aspect ratio of $M_{3a(b)}$ can be used to minimize the common mode gain.

The second gain stage operating in class AB is used to further enhance the overall gain of the system. Routine analysis shows that the second-stage gain is $(g_{m4a(b)}+g_{m5a(b)})(r_{o4a(b)}//r_{o5a(b)})$. The negative feedback is employed to ensure that the voltage at port X follows the voltage at port Y. Straightforward analysis shows that the impedance at port X is given by

$$R_x \approx \frac{1}{\left(g_{m4a(b)}+g_{m5a(b)}\right)g_{mbF1(2)}g_{m1a(b),2a(b)}R_{GF1(2)}R_{G1(2)}} \tag{2}$$

where g_{mb} and g_m are the bulk and gate transconductance, respectively. Finally, the gate voltage at the gates of $M_{4a(b)}$ and $M_{5a(b)}$ are applied directly to the gates of $M_{6a(b)}$ and $M_{7a(b)}$ respectively so that differential current at port X is transferred to port Z.

Common-mode rejection circuitry

Figure 3 shows the common-mode rejection circuitry. The circuit is used to further suppress the common-mode output signal. Bulk-driven fully differential pairs ($M_{8a(b)}$ and $M_{9a(b)}$) are employed and operate as a common-mode detector. Therefore, rail-to-rail operation at ports X is obtained. The operation of the circuit can be explained as follows. In case of differential input signals, there will be no current signal passing through M_{10a} nor M_{10b} and the output signal $v_{CMFB1a(b)}$ is nearly constant. Nevertheless, when the input signal is common-mode signal, the common-mode current is generated and passed to M_{10a} and $M_{11a(b)}$. Since $M_{11a(b)}$ is connected in the common source configuration, $v_{CMFB1a(b)}$ is out of phase with the input common mode voltage thus suppressing the common-mode gain.

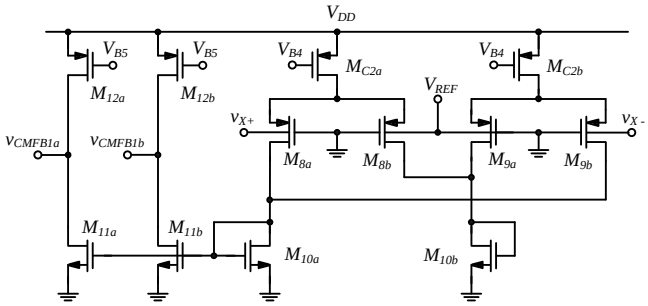


Fig. 3. Common-mode rejection circuitry [10].

SIMULATION RESULTS AND DISCUSSIONS

The proposed FDCCII is simulated with HSPICE using a 0.18 μm standard CMOS technology and 1 V supply voltage. The bias currents of the input and the output stages are 10 μA. Fig. 4(a) shows the DC voltage and current transfer characteristics between ports Y and X and ports X and Z, respectively. The result shows good linearity over a wide voltage range (-1V to 1V) with the total harmonic distortion less than 1.6 %. Fig. 5(a) shows the frequency response of the voltage transfer V_Z/V_X and current transfer I_Z/I_X characteristics which are close to 0 dB at low frequency with the bandwidth of 25.7 MHz and 30 MHz, respectively. The transient response of the FDCCII between the input voltage V_Y and output voltage V_X is illustrated in Fig. 5(b). A 2 V_{pp} sinusoidal wave at 1 MHz is applied to port Y. The result shows good voltage transfer over a wide input range.

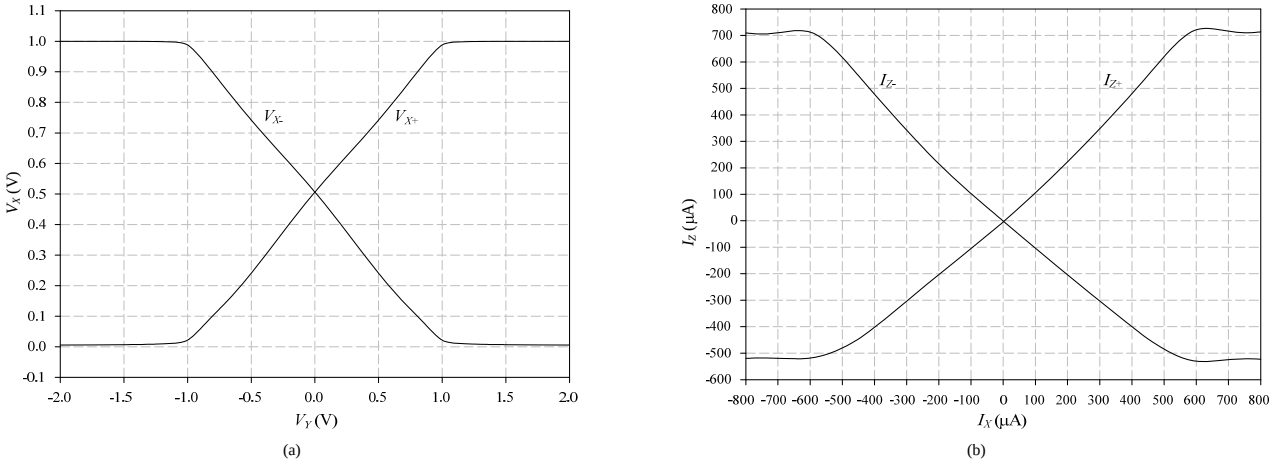
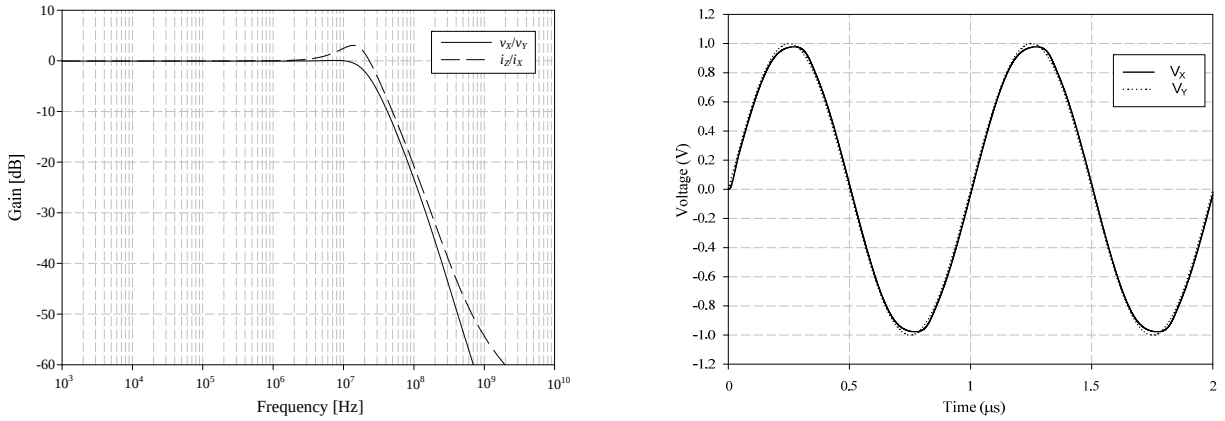


Fig. 4. (a) X-Y fully differential DC characteristic and (b) X-Z fully differential DC characteristic.



(a) (b)

Fig. 5. (a) Frequency response of v_X/v_Y and i_Z/i_X and (b) Transient response (Input 2 Vpp, 1 MHz).

CONCLUSIONS

A feedforward bulk-driven class AB fully-differential second-generation current conveyer (FDCCII) is presented. The circuit employs bulk-driven to achieve large input swing. The feedforward technique is also employed to increase and suppress the differential and common mode gains, respectively. Class AB output stage enhances the output current driving capability. The circuit shows good dc transfer characteristics with good linearity.

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