Low-Voltage Bulk-Driven QFG-Regulated Self-Cascode Super MOS Transistor

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***Abstract*—A bulk-driven super MOS transistor (BD-SMT) for low voltage operation is presented. The proposed transistor achieves a high effective transconductance ($G_{m(eff)}$), high effective drain impedance ($R_{D(eff)}$) and low effective source impedance ($R_{S(eff)}$). BD-SMT is designed based on regulated self-cascode and negative feedback techniques. The transistor been designed using a 0.18 μm CMOS technology and operated from a 0.4 V supply with a static power consumption of 12 μW. The simulation results showed higher $G_{m(eff)}$, larger $R_{D(eff)}$ and smaller $R_{S(eff)}$ as compared to those of simple bulk-driven MOS transistor.**

Keywords—low voltage; bulk-driven; regulated self-cascode.

I. INTRODUCTION

Metal-oxide semiconductor field-effect transistor (MOS transistor) is the most widely used device in both digital and analog integrated circuits. Main characteristics of MOSFET include, for example, high input impedance, ease of scaling and simple fabrication process.

Bulk-driven MOS transistor (BD-MT) has been proposed to design low voltage amplifiers with rail-to-rail input operation [1-2]. Main drawback of BD-MT is its low bulk transconductance (g_{mb}) [3-13]. As a result, the impedance looking into the source (R_S) is rather high since $R_S \propto 1/g_{mb}$. It is also known that the drain-to-source impedance of modern nanoscale MOSFET (R_D) is small due to short channel effect. Several super MOS transistors (SMTs) have been reported and they were developed based on the regulated cascade technique (RGC). The resulting SMTs demonstrated an enhanced effective drain resistance ($R_{D(eff)}$) [14-18].

A single stage common source (CS) amplifier using MOSFET operating in the weak inversion and a negative feedback technique was used to increase $R_{D(eff)}$ [14]. Its weak inversion operation allowed the rail-to-rail output swing. Improved SMTs using a high-gain feedback amplifier were also proposed [15, 16]. An enhanced loop gain resulted in very large $R_{D(eff)}$. In addition, the output swing showed rail-to-rail operation since PMOS was used in the feedback loop. It is however noticed that these SMTs required a minimum supply voltage of $4V_{DSAT} + 3V_T$ which is quite large. SMT using single-stage OTA, and a Miller amplifier was proposed. The transistor showed high speed and gain. [17].

Recently, SMT using a two stage cascade common source amplifier connected in a negative feedback configuration was reported [18]. The obtained SMT exhibited wide voltage swing, high effective transcondutance $G_{m(eff)}$, low source resistance $R_{S(eff)}$ and, in addition, can operate at low supply ($2V_{DSAT} + V_T$). Nevertheless, $R_{D(eff)}$ is equal to that of a conventional MOSFET (i.e., $R_{D(eff)} = r_o$). It is noted that all mentioned SMTs either achieved high $R_{D(eff)}$ or low $R_{S(eff)}$. Nonetheless, none of them achieved high $R_{D(eff)}$ and low $R_{S(eff)}$ at the same time. Moreover, supply voltages required were high and the input swing was limited mainly by V_T.

In this paper, low-voltage bulk-driven regulated self-cascode super MOS transistor (BD-SMT) is presented. The proposed BD-SMT demonstrates a high $G_{m(eff)}$, high $R_{D(eff)}$ and low $R_{S(eff)}$ simultaneously. The input swing at the bulk terminal shows rail-to-rail operation and the SMT can operate from a supply voltage as low as $V_T + V_{DSAT}$.

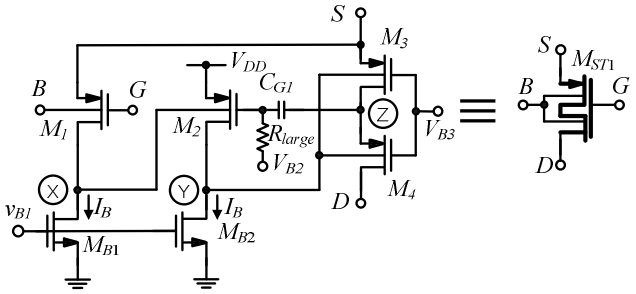

Fig. 1. Proposed super MOS transistor (BD-SMT).

II. PROPOSED BULK-DRIVEN SUPER MOS TRANSISTOR

Fig. 1 shows the proposed BD-SMT. $M_{B1} - M_{B2}$ operated as current sources to bias M_1 and M_2, respectively. M_1 and M_2 are connected as a bulk-driven CS amplifiers. M_3 and M_4 form self-cascode transistor. As will be described later, quasi-floating gate (QFG) transistor M_2 is used to increase $R_{D(eff)}$ while M_1 and M_2 are used to reduce $R_{S(eff)}$ and increase $G_{m(eff)}$.

The operation of BD-SMT can be explained as follows. If the test voltage (v_t) is applied to bulk of M_1, the signal v_t is amplified at node X. The amplified signal at node X is further amplified by common-source (CS) amplifier (M_2) at node Y which is then fed to the body of the self-cascade transistor M_3 and M_4 and finally converted into the drain current.

By using a typical small signal analysis, the effective transconductance ($G_{m(eff)}$) of BD-SMT can be shown as

$$G_{m(eff)} \cong \frac{g_{mb1}g_{mb2}g_{mb4}\left(r_{O1} \parallel r_{OB1}\right)\left(r_{O2} \parallel r_{OB2}\right)}{\left(g_{m4}+g_{mb4}\right)r_{O3(lin)}}, \quad (1)$$

where g_{mbi} and r_{Oi} are bulk transconductance and drain-to-source impedance of the i[th] transistor, respectively. $r_{O3(lin)}$ is the drain-to-source impedance of M_3 in the linear region.

From Eq. (1), one can see that $G_{m(eff)}$ in comparison with BD-MT is increased by a factor of $g_{mb1}g_{mb2}(r_{O1}//r_{OB1})(r_{O2}//r_{OB1})/(g_{m4}+g_{mb4})r_{O3(lin)}$.

To analyze the impedance at the drain terminal, one apply the test current i_t at the drain terminal and find the corresponding v_t at the drain terminal. $R_{D(eff)}$ is given by the ratio of v_t and i_t. It is noticed i_t is converted into voltage at node Z which is amplified by the CS amplifier via the QFG M_2. The amplified signal is negatively fed back to the bulk terminals of M_3 and M_4. This regulated cascade configuration helps increasing $R_{D(eff)}$. A straight forward small signal analysis shows $R_{D(eff)}$ as

$$R_{D(eff)} = \left[\left(C_{G1}/C_T\right)g_{m2}g_{mb4}\left(r_{O2} \parallel r_{OB2}\right)+g_{m4}\right]r_{O3(lin)}r_{O4}, \quad (2)$$

where C_{G1} is the coupling capacitor and C_T is the total gate capacitance of M_2.

One can see that $R_{D(eff)}$ in comparison with BD-MT is increased by a factor of $[(C_{G1}/C_T)g_{m2}g_{mb4}(r_{O2}//r_{OB2})+g_{m4}]r_{O3(lin)}$.

To analyze the impedance at the source terminal, one can apply v_t at the source terminal and find the associated i_t. As can been seen from Fig. 1, v_t is amplified by the CS amplifier M_1 at node X which is then further amplified by the CS amplifier M_2 at node Y. The signal at node Y is fed back to the body of the self-cascode M_3 and M_4. An increase in the body voltage helps increasing the source current, and finally lowering the effective source impedance ($R_{S(eff)}$). A straight forward small signal analysis shows $R_{S(eff)}$ as

$$R_{S(eff)} \cong \frac{\left(g_{m4}+g_{mb4}\right)r_{O3(lin)}}{\left(g_{m1}+g_{mb1}\right)g_{mb2}g_{mb4}\left(r_{O1} \parallel r_{OB1}\right)\left(r_{O2} \parallel r_{OB2}\right)}, \quad (3)$$

Notice that $R_{S(eff)}$ in comparison with BD-MT is reduced by a factor of $(g_{m4}+g_{mb4})/[(g_{m1}+g_{mb1})g_{mb2}g_{m4}(r_{O1}//r_{OB1})(r_{O2}//r_{OB2})$.

TABLE I. TRANSISTOR DIMENSIONS

Transistor	*W/L (μm/μm)*	*Transistor*	*W/L (μm/μm)*
M_1	52/0.5	M_4	82/0.5
M_2	52/0.5	M_{B1-3}	604/10
M_3	130/0.5		

III. SIMULATION RESULTS AND DISCUSSION

The proposed circuit has been designed and simulated using a standard 0.18 μm CMOS technology to verify its performance. The supply voltage is 0.4 V and the bias voltage at the body is set to 0.2 V. The bias current of every transistor is 10 μA. C_{G1} is 0.4 pF. Table 1 shows the size of transistors. Transistor M_1, M_2 and M_4 operate in the saturation region while M_3 operates in the linear region.

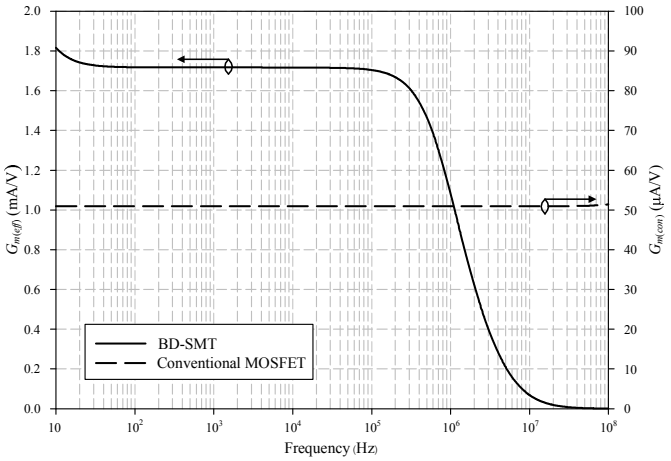

Fig. 2. $G_{m(eff)}$ versus $G_{m(con)}$.

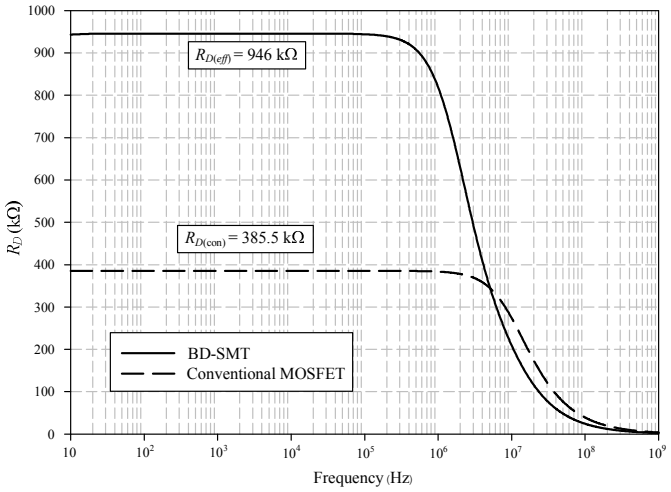

Fig. 3. $R_{D(eff)}$ versus $R_{D(con)}$.

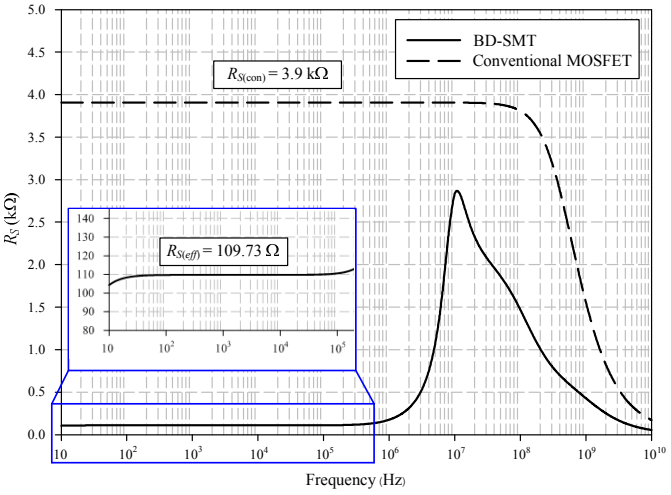

Fig. 4. $R_{S(eff)}$ versus $R_{S(con)}$.

Fig. 2 shows $G_{m(eff)}$ and the transconductance of the conventional BD-MT $G_{m(con)}$ for the same bias current and transistor size. As can be seen, $G_{m(eff)}$ is 1.72 mA/V while $G_{m(con)}$ reads only 50 μA/V (i.e., $G_{m(eff)}$ is around thirty times larger than $G_{m(con)}$).

$R_{D(eff)}$ versus the conventional drain impedance of BD-MT ($R_{D(con)}$) is shown in Fig. 3. As can be seen, $R_{D(eff)}$ is 946 kΩ while $R_{D(con)}$ reads 385.5 kΩ (i.e. $R_{D(eff)} \approx 2.5R_{D(con)}$). Fig. 4 shows $R_{S(eff)}$ of BD-SMT versus the source impedance of a BD-MT ($R_{S(con)}$). As can be seen, $R_{S(eff)}$ is 109.73 Ω while $R_{S(con)}$ is 3.9 kΩ (i.e. $R_{S(eff)} \approx 0.03R_{S(con)}$).

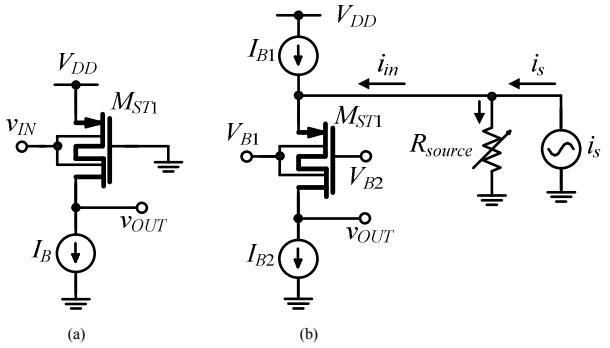

Fig. 5. (a) Common source and (b) common gate amplifiers.

To verify the performance of the proposed BD-SMT, BD-SMT is connected as a CS (Fig. 5a)) and common-gate (CG) (Fig. 5b)) amplifiers. Fig. 6 shows the frequency response using the proposed BD-SMT (solid line) and conventional MOSFET (dash line). The dc gains read 64.21 dB and 25.85 dB, respectively. Bandwidth of BD-SMT and conventional BD-SMT are 700 kHz and 10 MHz, respectively. The CS using BD-SMT has higher gain mainly due to an increase in both $G_{m(eff)}$ and $R_{D(eff)}$. Notes that an ideal current is used in the simulation since the MOSFET current source will affect the intrinsic gain and could mislead the result interpretation. Fig. 7 shows the transient response of the CS amplifier. A simple long channel MOSFET is used as a current source so that a realistic result is observed. As can be seen, CS amplifier exhibits a reasonable output voltage swing.

Fig. 8 shows the frequency response of the CG amplifier using the proposed BD-SMT (solid line) and the conventional MOSFET (dash line). The source impedance of the current source R_{source} is set equal to $R_{S(eff)}$ (i.e. R_{source} = 109.73 Ω). This leads to a current gain of 0.5. It is however noticed that the input current gain is reduced to only 0.012 when a conventional MOSFET is used mainly due to its higher source impedance $R_{S(con)}$. Fig. 9 shows the transient response of i_{in} when i_s is 4 μA_p sine wave at 20 kHz and R_{source} is R_{in}, $2R_{in}$ and $5R_{in}$. i_{in} is reduced to 2.04 μA_p, 2.7 μA_p and 3.35 μA_p, respectively.

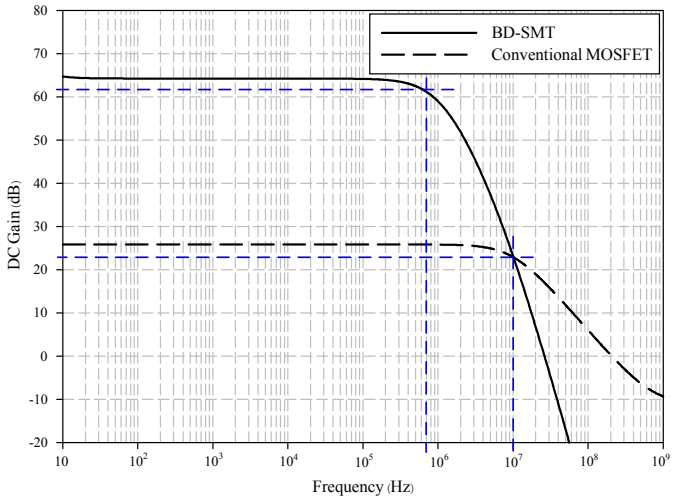

Fig. 6. Frequency response of Fig. 5a).

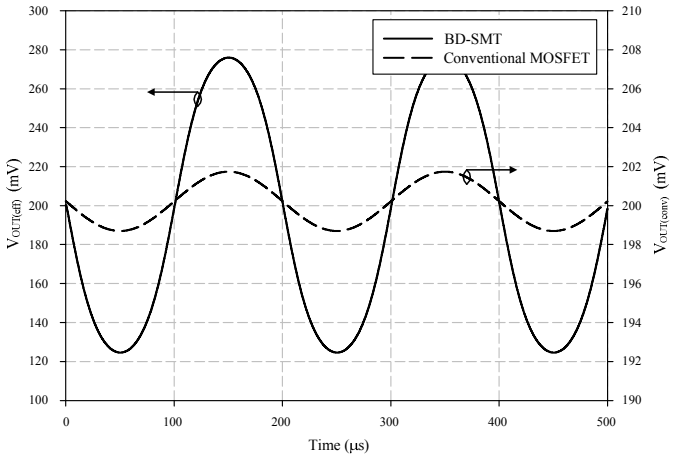

Fig. 7. Transient response of Fig. 5a).

Tables 2 shows a performance comparison of BD-SMT and other SMTs. Table 3 shows a comparison result between the proposed BD-SMT and conventional BD-MT.

TABLE II. PERFORMANCE COMPARISON BETWEEN THE BD-SMT AND OTHER REPORTED SMTS.

Parameter	V_{DD}	$G_{m(eff)}$	$R_{D(eff)}$	$R_{S(eff)}$
Conv	$V_{dsat} + V_T$	g_{m1}	r_{o1}	$1/g_{m1}$
[14]	$3V_{dsat} + 2V_T$	g_{m1}	$g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}$	$1/g_{m1}$
[15]	$3V_{dsat} + 3V_T$	g_{m1}	$g_{m2}r_{o1}r_{o2}g_{m5}g_{m6(7)}r_{o5(8)}r_{o6(7)}/2$	$1/g_{m1}$
[16]	$4V_{dsat} + 2V_T$	g_{m1}	$g_{m2}g_{m3}r_{o1}r_{o2}[r_{o3}//(r_{o8}+r_{o9})]$	$1/g_{m1}$
[17]	$4V_{dsat} + 2V_T$	g_{m1}	$g_{m2}g_{m3}g_{m6}r_{o1}r_{o2}(r_{o3}//r_{o4})\ (r_{o7}//r_{o9})$	$1/g_{m1}$
[18]	$2V_{dsat} + V_T$	$g_{m1}g_{m2}g_{m3}(r_{o1}//r_{oB1})(r_{o2}//r_{oB2})$	r_{o1}	$1\ /\ g_{m1}g_{m2}g_{m3}(r_{o1}//r_{oB1})(r_{o2}//r_{oB2})$
This work	$V_{dsat} + V_T$	$\frac{g_{mb1}g_{mb2}g_{mb4}\left(r_{O1} \parallel r_{OB1}\right)\left(r_{O2} \parallel r_{OB2}\right)}{\left(g_{m4}+g_{mb4}\right)r_{O3(lin)}}$	$[(C_{G1}/C_T)g_{m2}g_{mb4}\ (r_{o2}//r_{oB2}) + g_{m4})]r_{o3(lin)}r_{o4}$	$g_{mb5}r_{o3(lin)}\ /\ [(g_{m1}+g_{mb1})g_{mb2}(r_{o1}//r_{oB1}]$

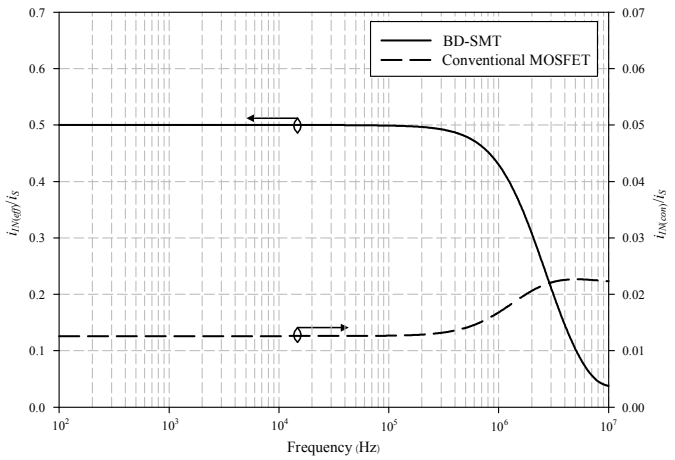

Fig. 8. Frequency response of Fig. 5b).

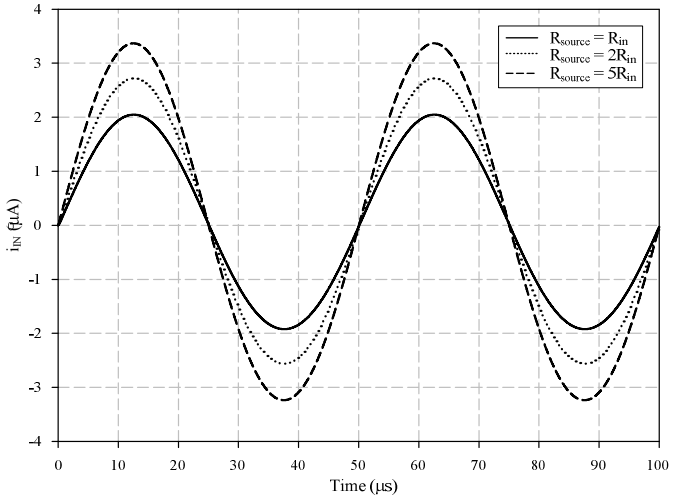

Fig. 9. Transient response of Fig. 5b).

TABLE III. PERFORMANCE COMPARISON.

Parameter	***Conventional***	***This work***
Supply voltage	0.4 V	0.4 V
The effective transconductance ($G_{m(eff)}$)	5 μA/V	1.72 mA/V
The effective drain impedance ($R_{D(eff)}$)	385.5 kΩ	946 kΩ
The effective source impedance ($R_{S(eff)}$)	3.9 kΩ	109.73 Ω
Unity gain frequency (f_T)	500 MHz	2.4 MHz
Power dissipasion	2 μW	12 μW

IV. CONCLUSIONS

In this paper, a low-voltage BD-SMT is presented. The BD-SMT is designed based on regulated-self cascade and negative feedback techniques. BD-SMT can operate at low supply and showed high effective transconductance ($G_{m(eff)}$), high effective drain impedance ($R_{D(eff)}$) and low effective source impedance ($R_{S(eff)}$).

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