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Trellis-Based Detecting the Insertion and Deletion Bits for Bit-Patterned Media Recording

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Abstract. Bit-patterned media recording (BPMR) is one of the promising technologies for realizing an areal density up to 4 Tb/in^2; however, it poses new challenges to read channel design, including the two-dimensional (2D) interference, media noise, and track mis-registration. Furthermore, the BPMR system encounters the insertion, deletion and substitution errors, which are primarily caused by mis-synchronization between the write clock and the island positions. In this paper, we propose a novel detection method that exploits the trellis structure to detect the occurrence of insertion/ deletion bits. Specifically, the specific marker bits are inserted periodically inside an input data sequence before recording onto a magnetic medium. Hence, the branch metric calculation is monitored during the marker bits to determine if there is any insertion/deletion error in the system. Numerical results indicate that the proposed method can performs better than the conventional one in terms of the percentage of detection and the percentage of missed detection and false-alarm, especially at low signal-to-noise ratio scenario.

Introduction

BPMR is an emerging technology for the next generation of hard disk drives, which can increase an areal density up to 4 tera bits per square inch (Tb/in^2) and beyond [1]. In BPMR, a data bit is stored in a single domain magnetic island surrounded by a non-magnetic material. At high-density BPMR, the spacing between data bit islands in both the along- and across-track directions is small, thus leading to the increase of 2D interference, media noise, and track mis-registration. Moreover, the BPMR system faces with the insertion/deletion (Ins/Del) and substitution errors. Specifically, the Ins/Del error is primarily caused by mis-synchronization between the write clock and the island positions, disk-speed variation, and head vibration [2], which are uncontrollable problems because of an imperfect mechanical system. Also, the substitution error is caused by the write head magnetic field not sufficient for changing the islands magnetic due to the switch field distribution (SFD). However, this paper focuses on how to detect the Ins/Del error. In general, the Ins/Del error is a challenging problem for BPMR because it can cause an error burst at data detection process, which cannot be handled by the conventional error-correction codes. Therefore, an efficient detection algorithm for the Ins/Del error is crucial for BPMR systems.

Recently, there are many works proposed to cope with the problem of Ins/Del errors in communi-cation channels. For example, Seller [3] introduced a so-called "marker" code to detect and correct the Ins/Del errors, whose encoding and decoding processes are performed, based on a look-up table. Ng *et al.* [2] presented a 2D code for correcting the Ins/Del errors in BPMR, which has high complexity and requires large memory. In addition, Kuznetsov and Erden [4] proposed to use the Levenshtein code to detect and correct the Ins/Del errors; however, this scheme is very sensitive to the substitution error. Finally, Koonkarnkhai *et al.* [5] presented an iterative decoding scheme to handle the Ins/Del error for BPMR, where the marker code and the VT code [6] are used to detect and correct the Ins/Del error, respectively.

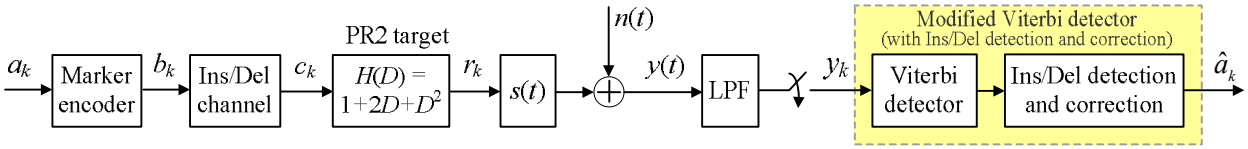

Fig. 1. A channel model with Ins/Del error.

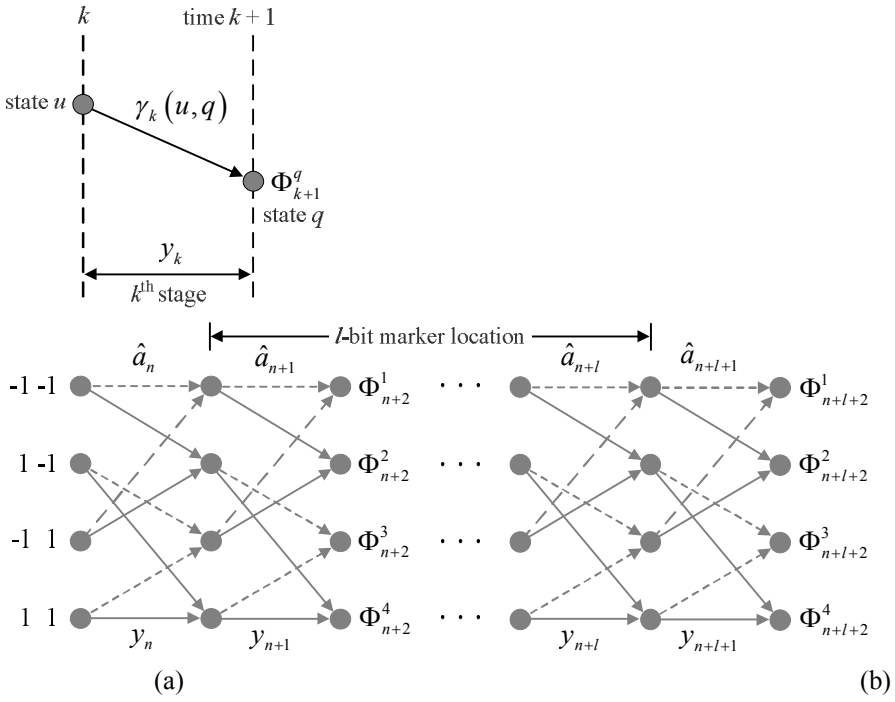

Fig. 2. (a) Trellis diagram and (b) trellis diagram for the PR2 target.

However, this paper focuses on detecting the Ins/Del error in BPMR systems. Since the trellis-based detector is employed to decode a received data sequence in BPMR systems, we exploit the trellis diagram to develop a method to detect the Ins/Del error.

Channel Model

Consider a perfectly equalized channel with Ins/Del error in Fig. 1. The marker bits [3] are first inserted periodically inside an input data sequence $a_k \in \{\pm 1\}$ with bit period T, which will

then be corrupted by the insertion or deletion error to obtain a sequence c_k. In this paper, we consider the case where the $(k+1)^{th}$ inserted bit is same as the k^{th} bit because a write clock of the k^{th} bit is spanned [2]. Hence, the readback signal can be written as

$$y(t) = \sum_k r_k s(t - kT) + n(t) \quad (1)$$

where $r_k = c_k * h_k$ is the noiseless channel output, $*$ is a convolution operator, $H(D) = \sum_{k=0}^{2} h_k D^k = 1 + 2D + D^2$ is the PR2 target, D is a unit delay operator, $s(t) = \sin(\pi t/T)/(\pi t/T)$ is an ideal zero-excess bandwidth Nyquist pulse, and $n(t)$ is an additive white Gaussian noise with two-sided power spectrum density $N_0/2$. The received signal $y(t)$ is filtered by an ideal lowpass filter (LPF), whose impulse response is $s(t)/T$, to get rid the out-of-band noise, and is sampled at time $t = kT$ assuming perfect synchronization. In a conventional setting, the sequence y_k is sent to the Viterbi detector (VD) followed by the Ins/Del detection and correction algorithm for the error to determine the most likely input sequence a_k.

Proposed Method

Fig. 2(a) shows the trellis diagram [7], where (u, q) denotes the transition from state u to state q, $\gamma_k(u, q)$ represents the branch metric associated with (u, q), and Φ_{k+1}^{q} is the sum of all branch matrices $\{\gamma_k(u,q)\}$ along the survival path that arrives in state q at time $k+1$. The proposed method employs the VD with a decoding depth of $(5L)T$ to decode a sequence y_k [7], where $L = 3$ is the PR2 target length. Also, we define $\hat{\mathbf{a}}_k^{k+m} = [\hat{a}_k, \hat{a}_{k+1}, \ldots, \hat{a}_{k+m}]$ as the set of decoded bits from time k to time $k+m$ obtained from the VD. Here, we propose to use the l-bit marker code of the form $\mathbf{M} = [1\ -1\ \ldots\ -1\ 1]$,

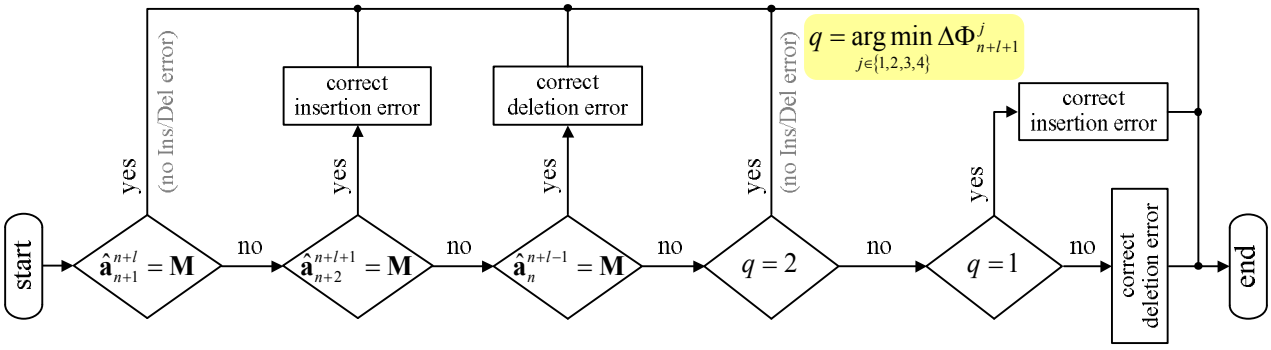

Fig. 3. Flowchart of the proposed method for combating one Ins/Del error.

i.e., there are $(l-2)$ bits of -1's between the bit '1', where $l \geq 2$. This l-bit marker code will be inserted at every n user data bits [4], where the length of one block code is $n + l$. Fig. 2(b) shows the trellis diagram for the PR2 target to explain how the proposed method operates.

This paper assumes that only one insertion or deletion error is occurred within one block code. To detect the Ins/Del error for each n-bit input data, we follow the flowchart illustrated in Fig. 3. First,

we compare $\hat{\mathbf{a}}_{n+1}^{n+l}$ and $\mathbf{M}$. If $\hat{\mathbf{a}}_{n+1}^{n+l} = \mathbf{M}$, it means no Ins/Del error in a system; otherwise, there might be an Ins/Del error. Specifically, the insertion error is detected if $\hat{\mathbf{a}}_{n+2}^{n+l+1} = \mathbf{M}$, whereas the deletion
error is present if $\hat{\mathbf{a}}_{n}^{n+l-1} = \mathbf{M}$. Nonetheless, if these three conditions are still not satisfied, we cannot conclude if the system encounters an Ins/Del error or not. Instead, we define the path metric difference at the end of the marker code according to

$$\Delta\Phi_{n+l+1}^{j} = \left|\Phi_{n+l+1}^{j} - \Phi_{n+1}^{i_{n+1}}\right|, \quad (2)$$

where $q \in \{1, 2, 3, 4\}$ and i_{n+1} is the beginning state at time $n+1$ associated with the survival path arriving in state j at time $n+l+1$. Let q denote the state that yields a minimum $\Delta\Phi_{n+l+1}^{q}$, i.e.,

$$q = \arg\min_{j\in\{1,2,3,4\}} \left\{\Delta\Phi_{n+l+1}^{j}\right\}. \quad (3)$$

With the proposed pattern of the l-bit marker code, i.e., $\mathbf{M}$ = [1 -1 ... -1 1], for the PR2 target, it is easy to use the state q to determine the Ins/Del error. Specifically, there is no Ins/Del error when $q = 2$; an insertion error is present when $q = 1$; and there is a deletion error when $q \in \{3, 4\}$.

Numerical Result

In simulation, the signal-to-noise ratio is defined as SNR = $10\log_{10}(\Sigma_k|h_k|^2/2R\sigma^2)$ in decibel (dB), where R is code rate and $\sigma^2 = N_0/(2T)$ is noise power. One input data sector contains 3840 bits and the l-bit marker code is inserted uniformly at every data block of $n = 256$ bits (some 256-bit data block contains one insertion or deletion error, but some does not. This paper makes a comparison between the conventional scheme using the 3-bit marker code from [3] with $R = 256/259$, and the proposed scheme with $R = 256/(256+l)$, where l is the length of the proposed marker code. To compare the performance, we use the percentage of detection (i.e., can detect the presence of an Ins/Del error), missed detection (i.e., cannot detect the presence of an Ins/Del error), and false alarm (i.e., no Ins/Del error but it said there is) as a criterion.

Fig. 4(a) compares the performance of the proposed scheme for different l's. Clearly, the higher the SNR, the higher the percentage of detection, and the lower the percentage of missed detection and false alarm. In addition, we found that the marker code of $l = 5$ bits is sufficient so as to maintain a high code rate. From now on, the 5-bit marker code [1 -1 -1 -1 1] will be employed in the proposed scheme when comparing its performance with the conventional scheme. Next, we compare the

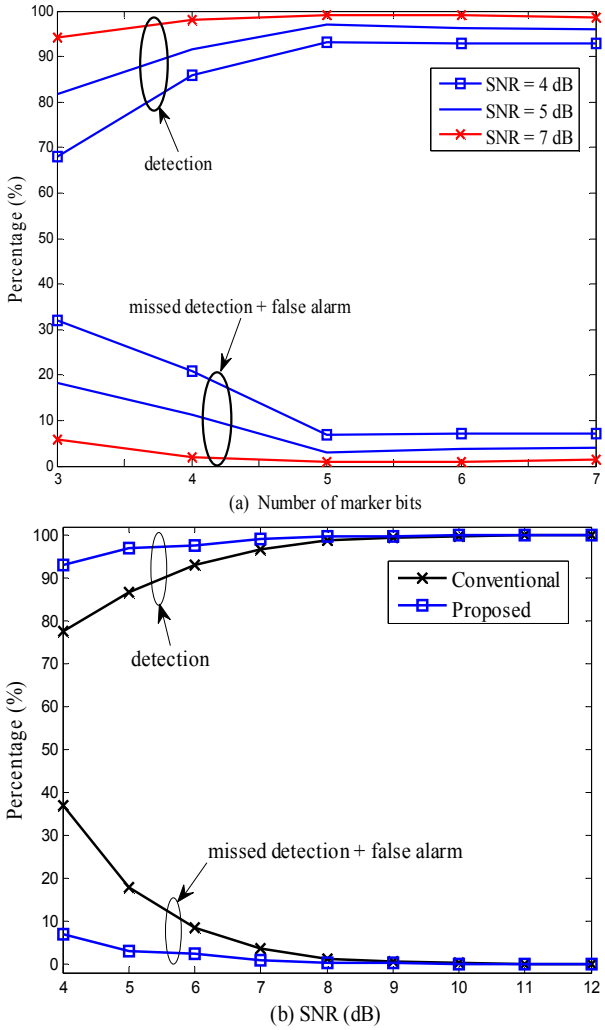

Fig. 4. (a) Performance of the proposed scheme as a function of the marker code lengths, and (b) performance comparison in terms of the percentage of detection and that of missed detection and false alarm.

performance of different schemes in Fig. 4(b). It is apparent that the proposed scheme performs better than the conventional scheme in terms of the percentage of detection and that of missed detection and false alarm, especially at low SNR. Therefore, it might be worth utilizing the proposed detection algorithm for the Ins/Del error in BPMR systems.

Summary

The insertion and deletion error is the challenging problem for the BPMR system because it can cause a burst error in the data detection process. A detection and correction algorithm for handling an Ins/Del error is essential for BPMR systems. This paper focuses only on how to detect the Ins/Del error efficiently. Thus, we propose the detection method for the Ins/Del error, which is performed on the trellis diagram. From the simulations, we found that the proposed detection method with the 5-bit marker code yields higher percentage of detection and lower percentage of missed detection and false-alarm than the conventional scheme that employs the 3-bit marker code. It should be noted that in general, the detection algorithm for the Ins/Del error is of importance because if we can detect it, we can then apply the correction

algorithm to solve the Ins/Del error, thus increasing the overall system performance. For the correction algorithm, we suggest a simple method to correct one Ins/Del error by discarding/inserting one dummy bit from/in the middle of the data block before re-decoding that data block (will be investigated further in our future work).

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